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Approved by:	RW E-KAZ

This document is valid for all SKiiP®3 V3 catalogue types as well as for customized SKiiP®3 V3 with restrictions according to the customer specification.
The document remains effective until replaced by a subsequent revision of this document.

Technical Explanation SKiiP®3 V3

Please note:
Unless otherwise specified, all values in this technical explanation are typical values. Typical values are the average values expected in large quantities and are provided for information purposes only. These values can and do vary in different applications. All operating parameters should be validated by user's technical experts for each application.
This document is valid for the entire catalogue SKiiP types with the delivery dates from 01.01.2012 ongoing. The document remains effective until replaced by subsequent revision of this document.

Table of Content

1. Related documents

- Data sheets SKiiP®3 V3
- Data sheet SKiiP®3 F-Option
- Technical Explanation SKiiP®3 F-Option
- Data sheets SKiiP®3 Parallel Board
- Technical Explanation SKiiP®3 Parallel Board

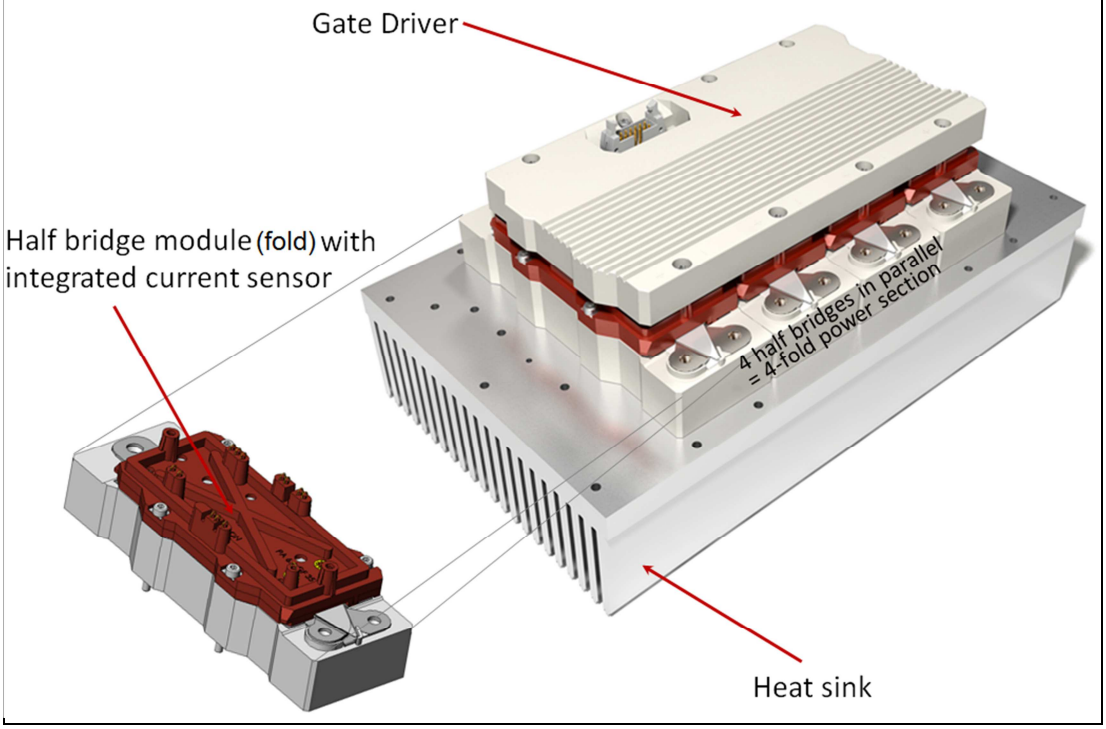
All these documents can be found on the SEMIKRON internet page.

2. Introduction

The 3rd generation SKiiP, by name SKiiP®3 V3, is an intelligent power module (IPM) with high power density and reliability. SEMIKRON´s SKiiP stands for “SEMIKRON intelligent integrated Power” which reveals that three matched components are integrated to one IPM:

- heat sinkpower section
- gate driver board
- IGBT half bridge “fold”

Figure 2.1: 4-fold SKiiP®3 V3



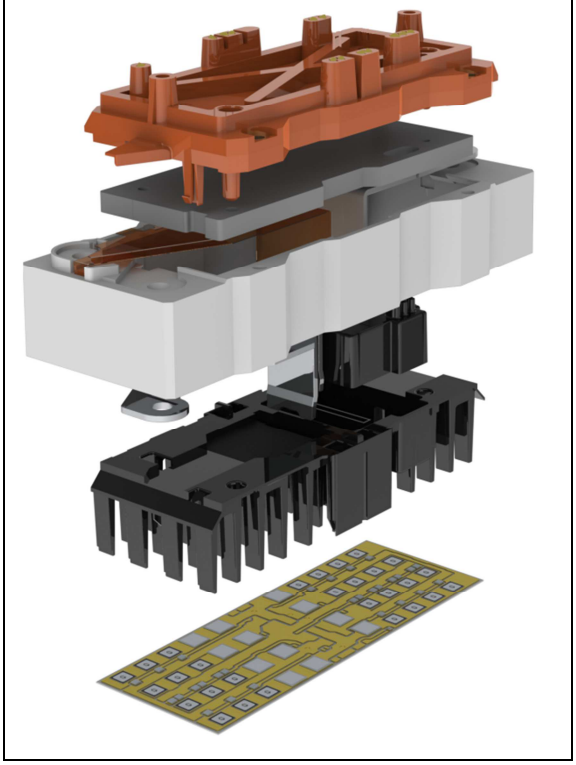
The power section consists of 2, 3 or 4 in parallel connected half bridge modules for a GB-type of the SKiiP3 or of 3 separetely controlled half bridge modules (1 half bridge per phase) for a GD-type.
A half bridge is indicated in Figure 2.2. The exploded view of half bridge module is shown in Figure 2.3.
The IGBT and the diode connected between DC+ terminal and AC terminal are named TOP IGBT / TOP diode. Consequently, the IGBT and the diode located between the AC and DC-terminal are named BOT IGBT / BOT diode.

Figure 2.2: Half bridge definition

In this document the following synonyms will be used for a power section with

- 2 half bridge modules in parallel = 2-fold
- 3 half bridge modules in parallel = 3-fold
- 4 half bridge modules in parallel = 4-fold

Figure 2.3: Half bridge “exploded view”



2.1 Heat sink

SEMIKRON offers highly efficient water cooled heat sinks and air cooled aluminium heat sinks to increase the performance of the IPM. Technical details of each type of heatsink can be found in the corresponding data sheets. Customer specified heat sinks can be assembled on request as well. However there are certain conditions for a successful heatsink customization, which should be considered to ensure that SEMIKRON can manufacture the IPM efficiently Please refer to PI 12-034 for additional information.

2.2 Power section

The SKiiP®3 V3 power section is based on the SKiiP pressure contact technology, which allows a compact power module design with very low thermal resistances, high thermal cycling capability and low parasitic stray inductances. The pressure contact technology facilitates that the Al_2O_3 or AlN DCB (direct copper bonded) substrate is pressed directly onto the heat sink without the use of a base plate. The pressure is induced by a pressure part on top, which is screwed to the heat sink.
Contact springs are used for all of the auxiliary contacts (gates, auxiliary emitters and temperature sensor). These spring contacts allow the solder-free connection of the driver PCB.

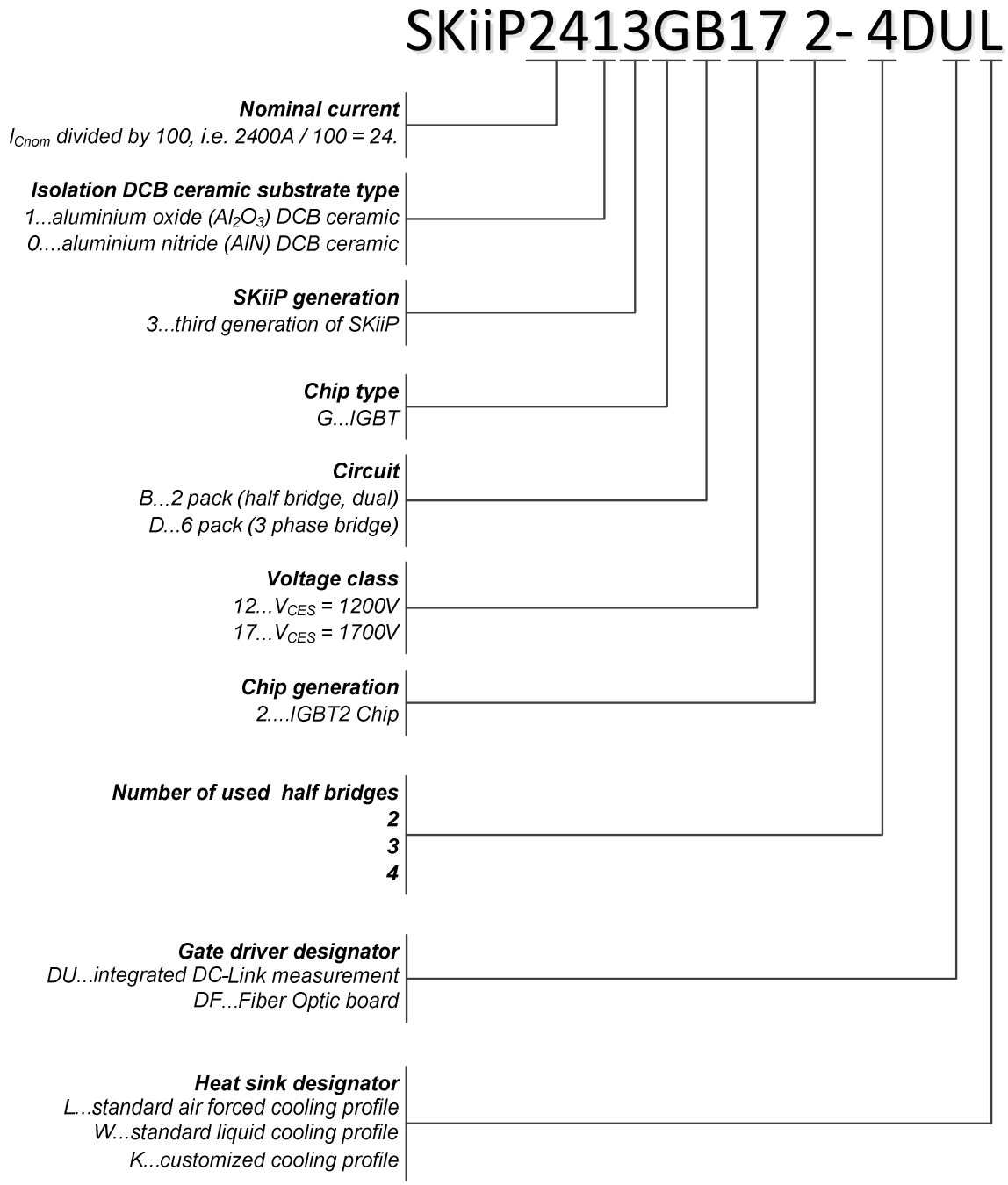
2.3 Gate Driver board

The task of the driver unit is both transferring incoming signals into powerful output signals to control the IGBTs and to ensure signal isolation between low and high voltage sides of the driver board. Additionally,

potential fault conditions are sensed and processed by the gate driver board to protect the power stage in case of a failure.
Additionally the SKiiP®3 provides the normalized analogue voltage signals of the actual AC-current value, the actual ceramic substrate temperature and the actual DC-Link voltage value (optional, depends on SKiiP®3 V3 type, please see Chapter 3, page 7 for the information). These signals are available at the SKiiP®3 V3 DIN41651 style gate driver connector for further use in the superimposed control unit.

3. Topologies and selection guide

3.1 Type Designation Code

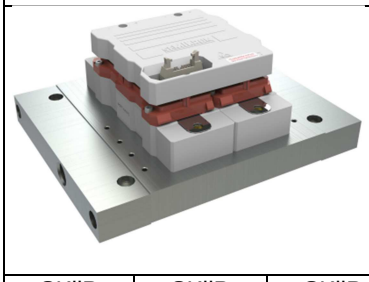
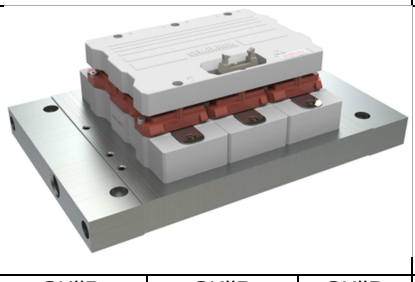
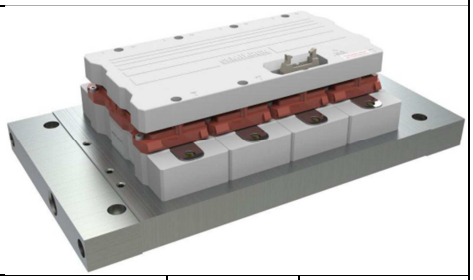
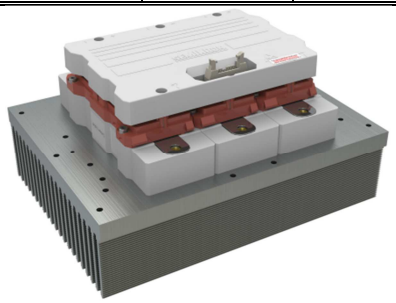
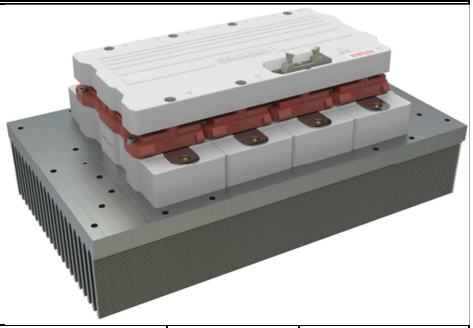
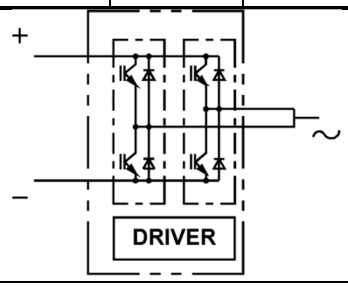
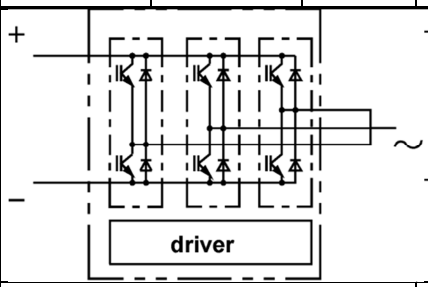
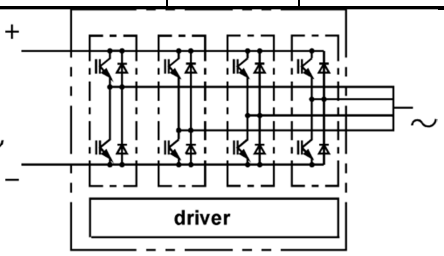


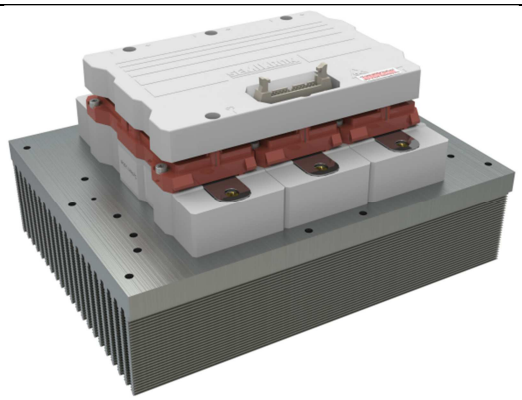
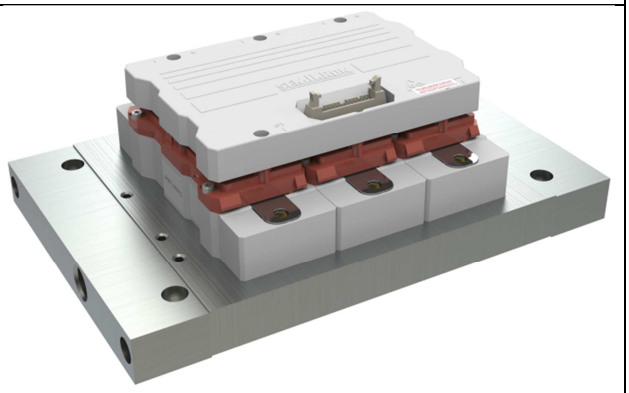
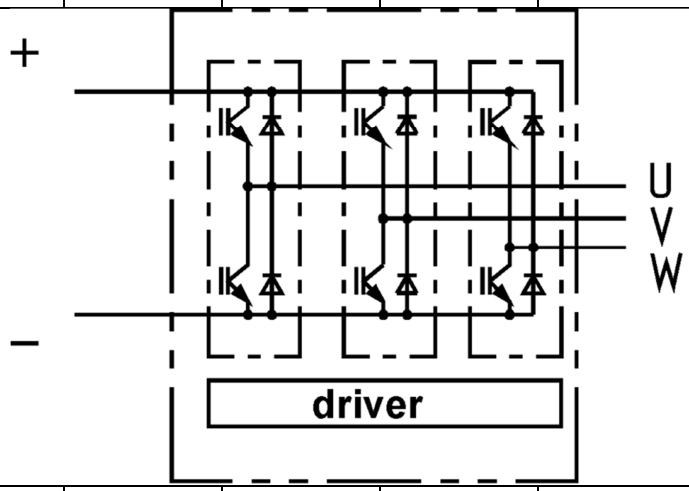
3.2 Overview of the available types and current ratings

Table 3-1 provides an overview of the available types and current ratings (I_{Cnom}).

Table 3-1: SKiiP®3 V3 standard product range

GB-Type (2-pack):

2-fold			3-fold			4-fold		
								
SKiiP 1213GB 123-2DW	SKiiP 1013GB 172-2DW	SKiiP 1203GB 172-2DW	SKiiP 1813GB 123-3DW	SKiiP 1513GB 172-3DW	SKiiP 1803GB 172-3DW	SKiiP 2413GB 123-4DW	SKiiP 2013GB 172-4DW	SKiiP 2403GB 172-4DW
								
SKiiP 1213GB 123-2DL	SKiiP 1013GB 172-2DL	SKiiP 1203GB 172-2DL	SKiiP 1813GB 123-3DL	SKiiP 1513GB 172-3DL	SKiiP 1803GB 172-3DL	SKiiP 2413GB 123-4DL	SKiiP 2013GB 172-4DL	SKiiP 2403GB 172-4DL
								
I_{Cnom} = 1000/1200A			I_{Cnom} = 1500/1800A			I_{Cnom} = 2000/2400A		

GD-Type (6-pack)							
							
SKiiP 603GD123-3DUL	SKiiP 613GD 123-3DUL	SKiiP 513GD172-3DUL	SKiiP 603GD172-3DUL	SKiiP 603GD123-3DUW	SKiiP 613GD 123-3DUW	SKiiP 513GD172-3DUW	SKiiP 603GD172-3DUW
							
I_{Cnom} = 600A	I_{Cnom} = 600A	I_{Cnom} = 500A	I_{Cnom} = 570A	I_{Cnom} = 600A	I_{Cnom} = 600A	I_{Cnom} = 500A	I_{Cnom} = 570A

For SKiiP®3 V3 there are two types of ceramic substrate available: Aluminum Nitrite (AlN) and Aluminum Oxide (Al_2O_3). AlN has got a better thermal conducivity than the Aluminum Oxide standard type which makes AlN eligible for the water cooled applications, whereas Al_2O_3 is basically utilized for the standard forced air cooled applications.

4. Standards and qualification tests

4.1 Tests for qualification and re-qualification

Table 4-1: SKiiP®3 V3 Tests for qualification and re-qualification

No	Test	Test Conditions	Standard
01	High Temperature Reverse Bias	500h, U_{DC}=1615V, V_{GE} = 0V, T_{jmax}=140°C	IEC 60747-9
02	High Temperature Gate Stress	500h, +/- V_{GSmax}/ V_{GEmax}, $T_C = T_{jmax} - 10°C$	IEC 60747-9
03	High Humidity High Temperature Reverse Bias	504h, 85°C, 85% RH, V_{CE} = 80% of V_{CEmax}, V_{GE} = 0V	IEC 60068 Part 2-67
04	High Temperature Storage	1000h, T_a= +125°C	IEC 60068 Part 2-2
05	Low Temperature Storage	1000h, T_a = -40°C	IEC 60068 Part 2-1
06	Thermal Cycling	100 cycles, -40°C/ +125°C	IEC 60068 Part 2-14
07	Power Cycling	20.000 load cycles @ ΔT_j = 110K, T_{jm}=95°C	IEC 60747-9
08	Vibration	Sinusoidal Sweep, 5g, x, y, z – axis, 2h/ axis	IEC 60068 Part 2-6
09	Shock	Halfsinusoidal Pulse, 30g, +/- x, +/- y, +/- z direction, 1000 times/ direction	IEC 60068 Part 2-27

4.2 Electromagnetic compatibility (EMC)

The SKiiP®3 is designed to comply with the following immunity tests with EMC compliant installation:

Table 4-2: SKiiP®3 V3 Electromagnetic compatibility

Immunity test	Conditions	Test level
Fast transients (Burst) (61000-4-4)	On driver board interfaces	4kV / 5kHz
Radio Frequency Fields (61000-4-3)	Polarisation: vertical + horizontal Frequency: 80 MHz - 1000 MHz Modulation: 80% AM, 1kHz Far field, homogeneous	 15V/m
RF Conducted Disturbance (61000-4-6)	Frequency: 150 kHz - 80 MHz Modulation: 80 % AM, 1kHz	20V
Electrostatic discharge (ESD) EN 61000-4-2	Contact discharge	8kV

4.3 Isolation coordination

The isolation of the SKiiP®3 V3 is designed according to EN50178.

Safety advice: The isolation of the temperature signal is a basic isolation only. In a failure case the plasma of an arc can apply high potential to the temperature sensor. Equipment which is designed for reinforced isolation must have additional isolation for all parts which might be touched by a person.

For working conditions please refer to the datasheet SKiiP®3 V3, p.3.

Table 4-3: Isolation limits SKiiP®3 V3

Isolation / Test level	Min value
Partial discharge extinction voltage (IEC60664-1) between high voltage and low voltage side of signal and power transformer	1700V_{rms}; Q_{PD} < 10pC
Rated impulse voltage (IEC60664-1) high voltage to low voltage and low voltage to heat sink	8kV 1,2/50µs

4.4 Installation altitude

The SKiiP®3 V3 is designed for overvoltage category III and for altitudes of up to 2000m.
The required clearance distances between mains-circuits and their environment for overvoltage category III are listed in EN50178.
For an earthed-neutral system the rated isolation voltage is defined in chapter 5.2.16.1 of EN50178 as:
"…the peak value of the rated voltage between phase and earthed neutral point."
Based on this standard the rated isolation voltage in case of a grounded delta grid (Figure 4.1) and a star grounded grid (Figure 4.2) can be derived as:
Rated isolation voltage in case of 690V grounded delta grid: 690V
Rated isolation voltage in case of 690V star grounded grid: 400V

Figure 4.1: Grounded delta grid

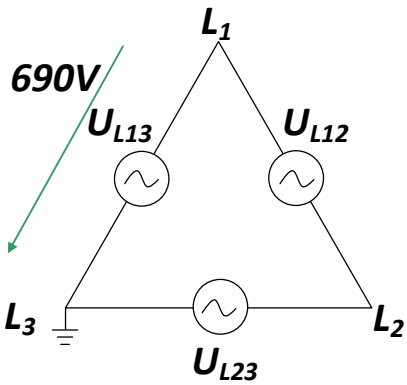
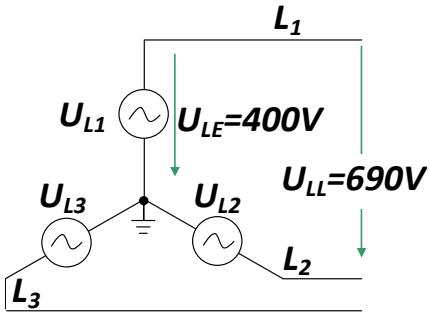


Figure 4.2: Star grounded circuit network (690V-TN-grid)



Based on the type of grid and the voltage level the required clearance distances for basic and reinforced isolation differ from the designed ones.
According to HD625 S1 and IEC60664-1 the maximum altitude can be calculated based on the factors between required and designed clearance distances.

Table 4-4: Altitude correction factors (IEC 60664-1)

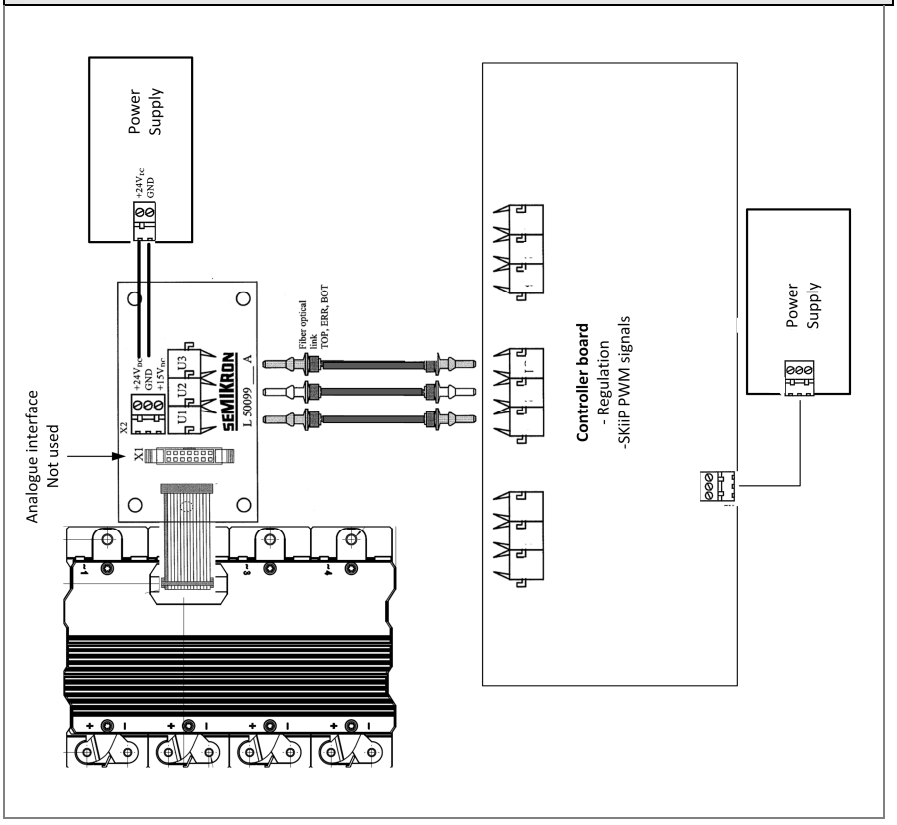
Altitude	Normal barometric pressure	Multiplication factor for clearances
m	kPa	
2 000	80,0	1,00
3 000	70,0	1,14
4 000	62,0	1,29
5 000	54,0	1,48
6 000	47,0	1,70

7 000	41,0	1,95
8 000	35,5	2,25
9 000	30,5	2,62
10 000	26,5	3,02
15 000	12,0	6,67
20 000	5,5	14,5

The overvoltage category influences the installation altitude too. To increase the altitude further the overvoltage category needs adjustment (EN50178):
"As an alternative to the values of table 3, columns 2 to 5, the clearances between mains-circuits of an EE and its environment may be designed in accordance with overvoltage category II, if facilities are provided which reduce overvoltages of category III to values of category II…However for reinforced isolation according to column 7 shall ***not*** *be reduced."*
The required clearance distances between mains-circuits and their environment for overvoltage category II are listed in EN50178.
If safety isolation is necessary the maximum altitude of SKiiP®3 V3 is 2857m (independent from an overvoltage category).
If only basic isolation is required even higher altitudes are possible. In case of a 690V TN grid and an overvoltage category II an altitude of theoretically 8305m for SKiiP®3 V3 is possible.
This is the case when an additional basic isolation is implemented between SKiiP driver interface and controller board. This can be realized by the following means (ref: Figure 4.3):

- Use of fiber optic for control signals (TOP, BOT, Error) and
- SKiiP analogue signals (current, DC-voltage and temperature measurement) are not used and
- all SKiiPs are individually supplied by separate power supplys to which no other circuit is connected.

Figure 4.3: Implementation of an additional basic isolation between SKiiP®3 V3 driver interface and controller board

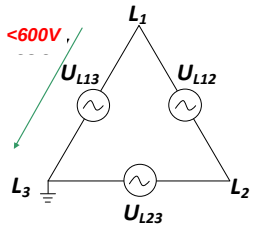
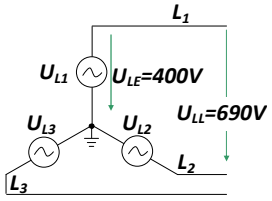
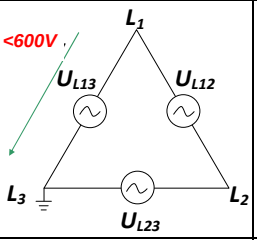
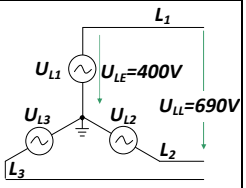


Finally, the installation altitude of SKiiP depends on:

- The type of grid (star grounded grid, delta grounded grid)
- The voltage level of the line to earth voltage (rated isolation voltage)
- The overvoltage category (II or III)
- Whether safety isolation is required or not

Table 4-5 summarizes the installation altitudes for SKiiP®3 V3.

Table 4-5: Installation altitudes for SKiiP®3 V3 in dependency on type of grid, overvoltage category and kind of required isolation

SKiiP®3 V3 (with 600V grounded delta)		Overvoltage category III		Overvoltage category II	
		Grounded delta grid	TN 690V	Grounded delta grid	TN 690V
					
Basic isolation to ground	**Required for 2000m**	5,5 mm	5,5 mm	3 mm	3 mm
	Existing	7,1 mm			
	Factor	1,29	1,29	2,36	2,36
	Altitude	**4000m**	**4000m**	**8305m**	**8305m**
Reinforced isolation	**Required for 2000m**	8 mm	8 mm	8 mm	8 mm
	Existing	9 mm			
	Factor	1,12	1,12	1,12	1,12
	Altitude	**2857m**	**2857m**	**2857m**	**2857m**
Maximum altitude with safety isolation		**2857m**	**2857m**	**2857m**	**2857m**
Maximum altitude without safety isolation		**4000m**	**4000m**	**8305m**	**8305m**

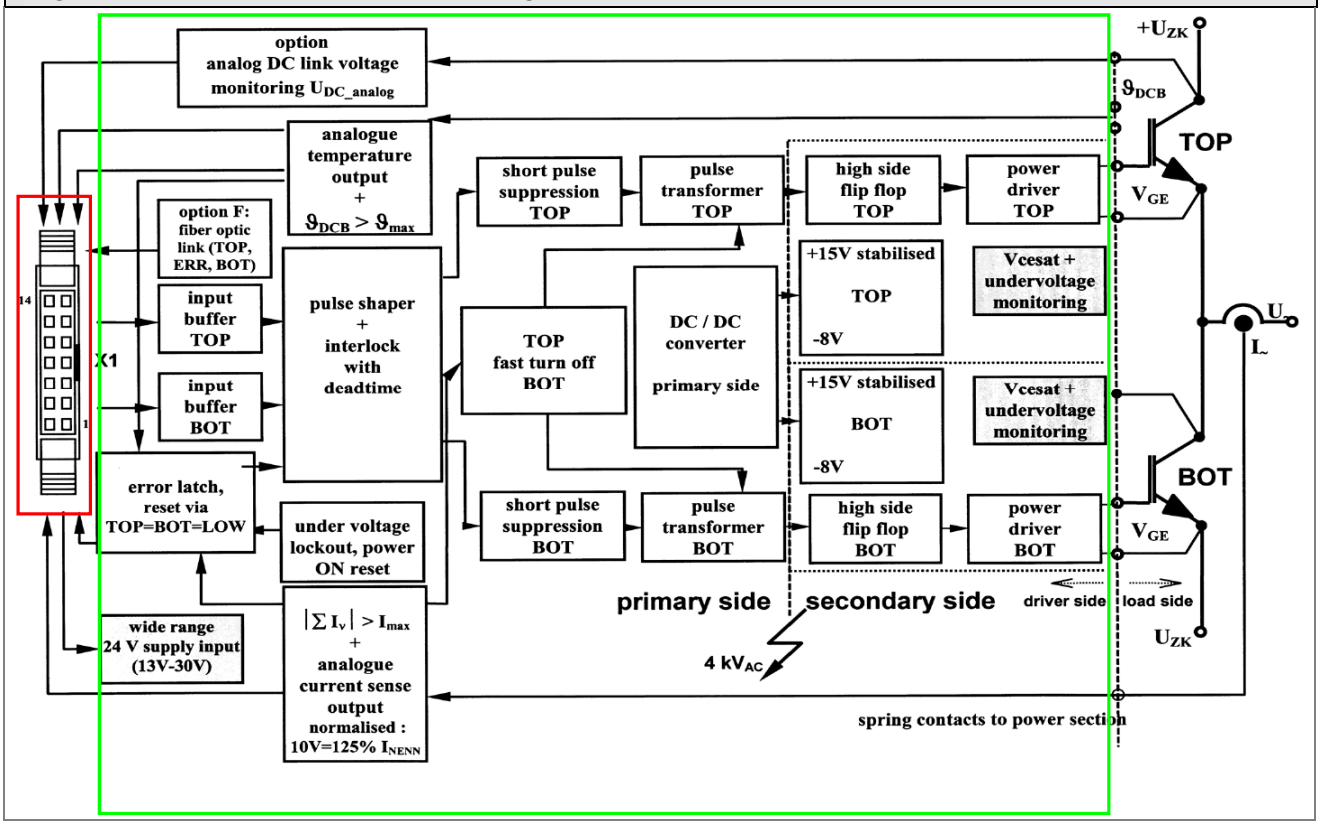
5. Gate Driver Board

5.1 Overview

The functionality of the Gate Driver can be seen in following block diagram.

- SKiiP®3 V3 DIN41651 gate driver connector, red block in Figure 5.1 (refer to Chapter 5.2)
- Gate driver board, green block in the Figure 5.1 (refer to Chapter 5.3)

Figure 5.1: Gate Driver Board block diagram



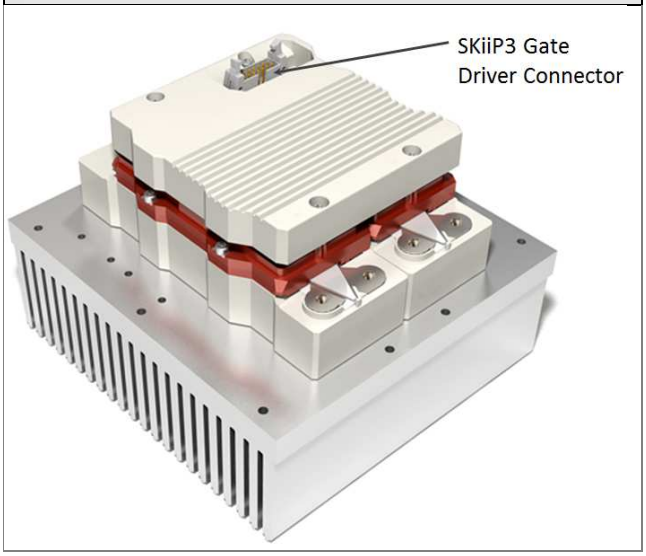
5.2 Gate driver interface

5.2.1 Overview

The gate driver interface of the SKiiP®3 V3 DIN41651 is marked in Figure 5.2. It is a 14 pin (GB-Type) or 26 pin (GD-Type) plug connector. The picture, the pin-out and the dimensions are summarized in Figure 5.3 for GB-Type and Figure 5.4 for GD-Type.
The connector includes pins for:

- External Power Supply (refer to chapter 5.2.3)
- Switching signal input (refer to chapter 5.2.4)
- Analogue signal outputs (refer to chapter 5.2.5)
- Error outputs (refer to chapter 0)
- 15V output for external components (refer to chapter 5.2.3)

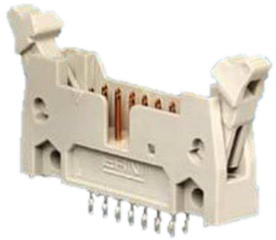
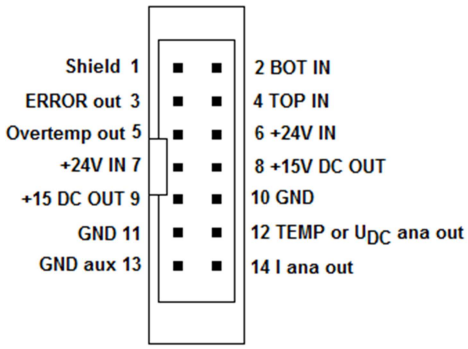
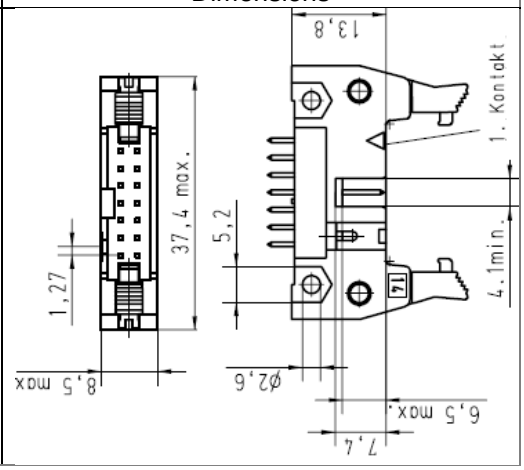
Figure 5.2: Gate Driver Interface



Magnetic transformers are used for isolation between gate driver low voltage and high voltage sides. The circuit used for the DC-Link voltage measurement is designed, manufactured and tested according to reinforced isolation standards (EN50178). The temperature sensor is functionally isolated on the ceramic substrate. Please see the datasheet SKiiP®3 V3, page 3 for detailed Isolation Coordination information.

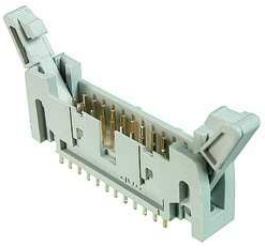
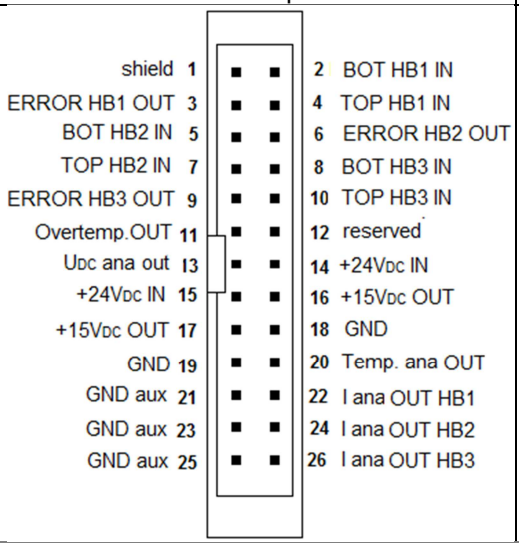
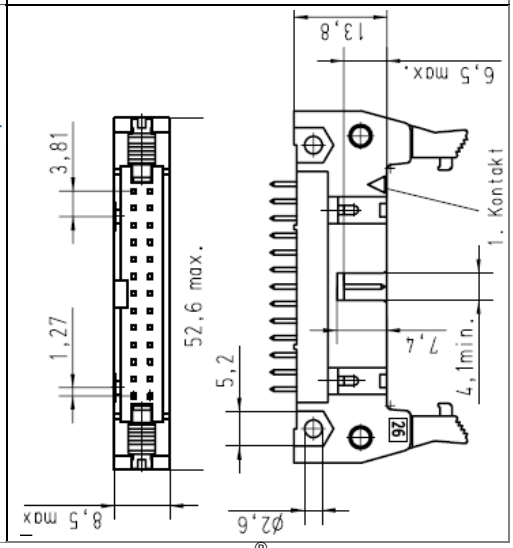
Safety advice: The isolation of the temperature signal is a basic isolation only. In a failure case the plasma of an arc can apply high potential to the temperature sensor. Equipment which is designed for reinforced isolation must have additional isolation for all parts which might be touched by a person.

Figure 5.3: SKiiP®3 V3-connector DIN41651, GB Type, male plug, vertical, top view

Picture	Pin Description	Dimensions
		

Pin 1 is marked with a triangle symbol (see the Figure 5.3, right) both on the male and female connectors.

Figure 5.4: SKiiP®3 V3-connector DIN41651, GD Type, male plug, vertical, top view

Picture	Pin Description	Dimensions
		

The following constraints of the cabling should be considered when connecting the SKiiP®3 V3 to a control system:

- The cable length should be kept shorter than 3m
- Longer cables must be shielded accordingly. The shield should be connected to pin 1 of the driver interface additionally

A verification according to mechanical stability and EMC behaviour in customer's application is necessary.

Please note: Do not remove the plug with applied voltage of the power supply. This can lead to unspecified voltage levels on the driver with the risk of damage or destruction.

5.2.2 Pin description

Table 5-1: Pin description SKiiP®3 V3 GB-Type

PIN	Signal	Function	Specification
1	Shield		
2	BOT IN	Switching signal input for low side IGBT	positive 15V CMOS logic; 10 kOhm impedance For more details see Chapter 5.2.4
3	ERROR OUT	Error signal	LOW = NO ERROR; open collector output For more details see Chapter 0
4	TOP IN	Switching signal input for high side IGBT	positive 15V CMOS logic; 10 kOhm impedance For more details see Chapter 5.2.4
5	Overtemp. OUT	Overtemperature error	LOW = NO ERROR; open collector output For more details see Chapter 0
6	+ 24 VDC IN	Wide range Power Supply	13V… 30V For more details see Chapter 5.2.3
7			
8	+ 15 VDC OUT	15V output for external components	50mA load For more details see Chapter 5.2.3
9			
10	GND	Power ground	
11			
12	Temp. ana OUT or U_{DC} ana OUT	Temperature signal out or DC-Link voltage out	For more details see Chapter 5.2.5 and data sheets SKiiP®3 V3, page 2
13	GND aux	Reference for analogue output signals	
14	I ana OUT	Current sensor out	For more details see Chapter 5.2.5 and data sheets SKiiP®3 V3, page 2

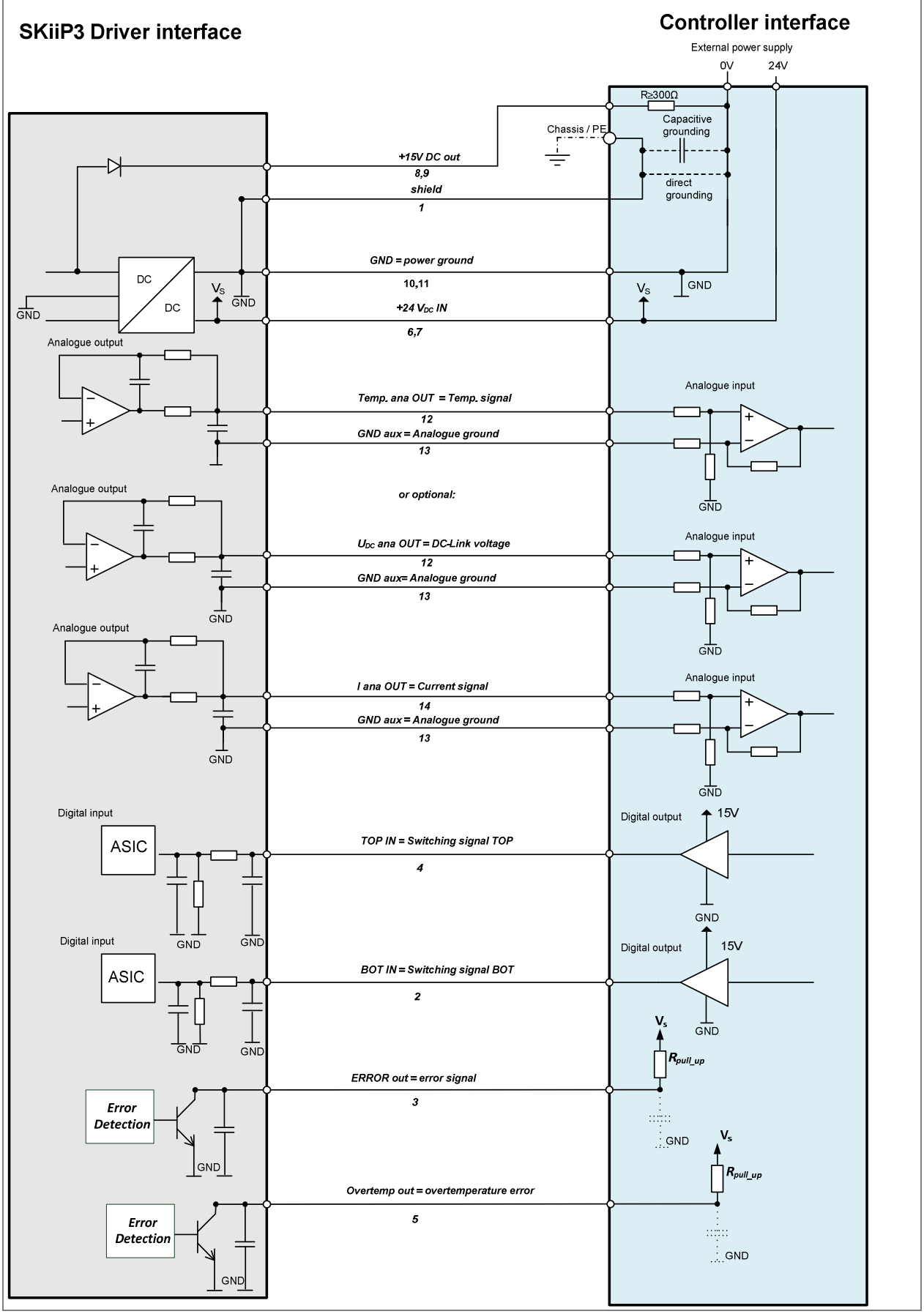
Table 5-2: Pin description SKiiP®3 V3 GD-Type

PIN	Signal	Function	Specification
1	Shield		
2	BOT HB1 IN	Switching signal input for low side IGBT phase U (half bridge1)	positive 15V CMOS logic; 10 kOhm impedance For more details see Chapter 5.2.4
3	ERROR HB1 OUT	Error signal phase U (half bridge1)	LOW = NO ERROR; open collector output For more details see Chapter 0
4	TOP HB1 IN	Switching signal input for high side IGBT phase U (half bridge1)	positive 15V CMOS logic; 10 kOhm impedance For more details see Chapter 5.2.4
5	BOT HB2 IN	Switching signal input for low side IGBT phase V (half bridge2)	positive 15V CMOS logic; 10 kOhm impedance For more details see Chapter 5.2.4
6	ERROR HB2 OUT	Error signal phase V (half bridge2)	LOW = NO ERROR; open collector output For more details see Chapter 0
7	TOP HB2 IN	Switching signal input for high side IGBT phase V (half bridge2)	positive 15V CMOS logic; 10 kOhm impedance

			For more details see Chapter 5.2.4
8	BOT HB3 IN	Switching signal input for low side IGBT phase W (half bridge3)	positive 15V CMOS logic; 10 kOhm impedance For more details see Chapter 5.2.4
9	ERROR HB3 OUT	Error signal phase W (half bridge 3)	LOW = NO ERROR; open collector output For more details see Chapter 0
10	TOP HB3 IN	Switching signal input for high side IGBT phase W (half bridge 3)	positive 15V CMOS logic; 10 kOhm impedance For more details see Chapter 5.2.4
11	Overtemp. OUT	Overtemperature error	LOW = NO ERROR; open collector output For more details see Chapter 0
12	reserved		
13	U_{DC} ana OUT	DC-link voltage out	For more details see Chapter 5.2.5 and data sheets SKiiP®3 V3, page 2
14	+ 24 VDC IN	Wide range Power Supply	13V… 30V For more details see Chapter 5.2.3
15			
16	+ 15 VDC OUT	15V output for external components	50mA load For more details see Chapter 5.2.3
17			
18	GND	Power ground	
19	GND	Power ground	
20	Temp. ana OUT	Temperature signal out	For more details see Chapter 5.2.5 and data sheets SKiiP®3 V3, page 2
21	GND aux	Reference for analogue output signals	
22	I ana OUT HB1	Current sensor out phase U	For more details see Chapter 5.2.5 and data sheets SKiiP®3 V3, page 2
23	GND aux	Reference for analogue output signals	
24	I ana OUT HB2	Current sensor out phase V	For more details see Chapter 5.2.5 and data sheets SKiiP®3 V3, page 2
25	GND aux	Reference for analogue output signals	
26	I ana OUT HB3	Current sensor out phase W	For more details see Chapter 5.2.5 and data sheets SKiiP®3 V3, page 2

In Figure 5.5 the left side of the diagram shows the equivalent circuit diagram of the driver board “GB-topology” with ground connections. The right side shows an application example for the controller side. The circuit diagram of the driver board “GD type” is correspondingly splitting the switching signal inputs and error outputs for each phase accordingly.

Figure 5.5: Overview schematics SKiiP®3 V3 interface, GB-Topology



5.2.3 External Power Supply

Table 5-3 shows the required features of an appropriate external power supply for a SKiiP®3 V3. All values are related to one SKiiP. In case the gate driver is supplied with supply voltage >15V it is possible to use 15V provided at the DIN 41651 connector of the gate driver as an external power supply, e.g. for a level shifter at the controller's output signals.

Table 5-3: Requirements to the external power supply	
Unregulated 24V power supply	The maximum ratings for the supply voltage are given in the SKiiP®3 V3 data sheet on page 1 (refer to symbol V_s). The supply voltage is defined at the SKiiP®3 V3 input, not at the controller output (consider voltage drop on connection cable)
I_{OUT} 15V (can be used if V_{DCin} >15V)	<50mA
Maximum rise time of 24V	<2 s
Rated current	1,5 times of the maximum driver input current
Minimum peak current	2 times of the maximum driver input current (At least 1,5A)
Please note: Do not apply switching signals during power on reset.	

The external power supply requires the capability to feed a minimum inrush current into the SKiiP at start-up of the system without entering a fault state itself. Typically power supplies with fold-back characteristic or hiccup-mode can create problems if insufficient over current margin is available. The voltage at the terminals of the SKiiP has to rise continuously and without any plateau formation.
In order to ensure continuous operation and to have sufficient margin in case of overload it is recommended to chose the rated current of the external power supply 50% higher than the maximum driver input current rating (see symbol I_s on page 2 of the corresponding SKiiP®3 V3 datasheet). The rated peak current of the supply must fulfill the specification as stated in Table 5-3.
If the power supply is able to provide a higher current, a peak current will flow in the first instant to charge up the input capacitances on the control board. The peak current value will be limited only by the external power supply and the effective impedances (e.g. cabling impedance). It is recommended to avoid paralleling of several external power supply units. Their different current limitations may lead to drops in the supply voltage and unpredictable instable behaviour.
The formula given in the SKiiP®3 V3 datasheet for calculating the supply current I_S (page 2) assumes a supply with 24V. The equation consists of three parts:
The first part, I_{S0}, is the current consumption of the driver during standby. No switching signals are applied. Consequently, no AC-current is flowing. Example below: SKiiP2413GB123 (I_{SO}=330mA)
The second part, k_1*f_{sw}, is the required current consumption of the driver in switching mode.
The third part, $k_2*I_{AC}^2$, is the current consumption required by the integrated current sensor to compensate the actual value of the AC-current.

$$I_{S0} + k_1 \cdot f_{sw} + k_2 \cdot I_{AC}^2$$

- $k_2 \cdot I_{AC}^2$: Current consumption of integrated current sensor
- $k_1 \cdot f_{sw}$: Current consumption of driver in switching mode
- I_{S0}: Standby current consumption of the driver

5.2.4 Switching Signal Inputs

The switching signal inputs TOP IN for the TOP and BOT IN for the BOT IGBT have a digital positive / active high logic (input HIGH = IGBT on; input LOW = IGBT off) characteristic.
For driving the inputs TOP IN and BOT IN it is mandatory to use line drivers that switch between 15V and 0V. Pull up and open collector output stages must not be used for driving these inputs.

Please note: A non connected input will be considered as LOW signal.

Figure 5.6: TOP/BOT PWM Signal Input GB-type

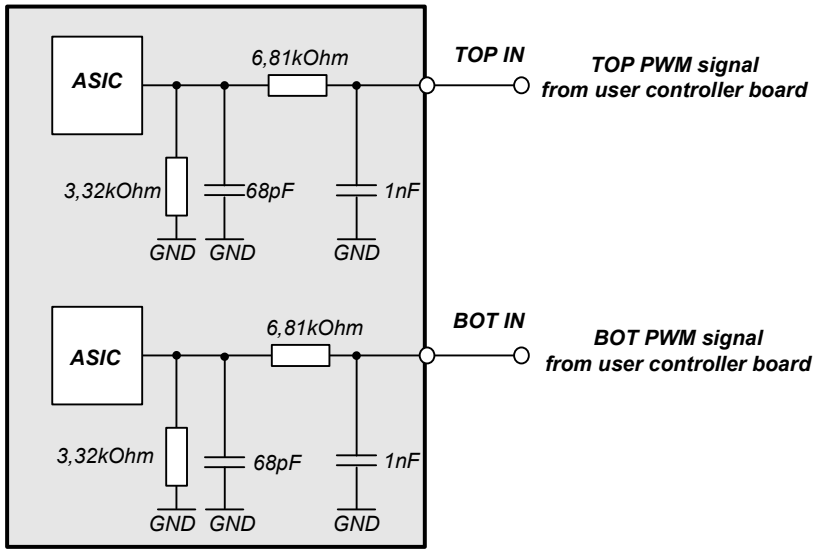
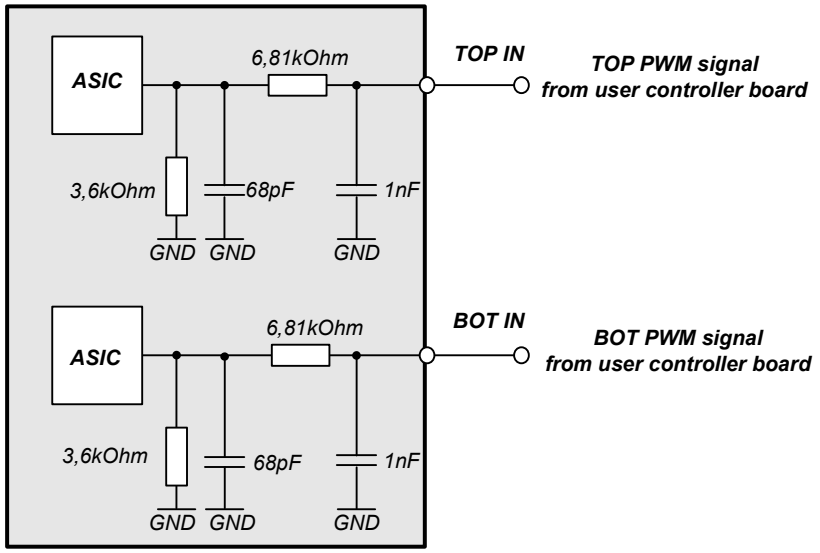


Figure 5.7: TOP/BOT PWM Signal Input GD-type

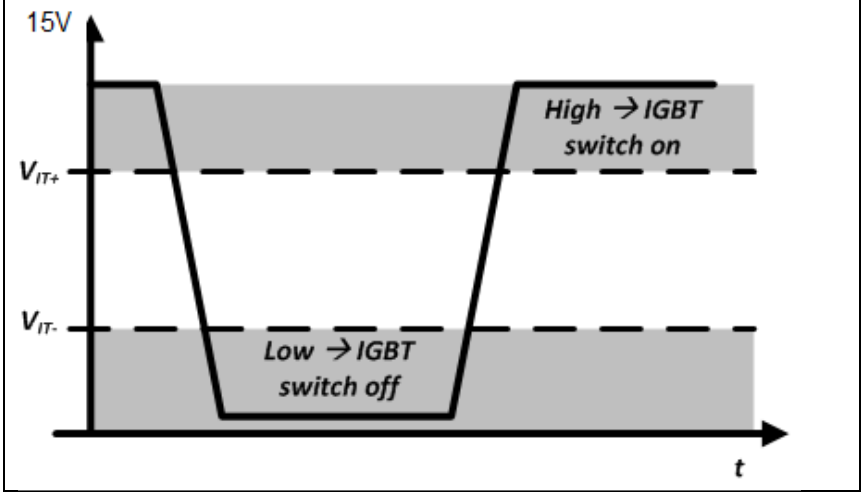


A 1nF capacitor is connected to the switching signal input to obtain high noise immunity. This capacitor can cause a delay of few ns for current limited line drivers, which can be neglected.
The choice of a line driver according to the demanded length of the ribbon cable is recommended. It is compulsory to use circuits which switch actively (push-pull) to +15V and 0V. Pull up and open collector output stages must not be used for TOP/BOT control signals.
The input resistance of the TOPin and BOTin terminal is about 10kOhm.

As shown in **Figure 5.8**. the switching signal will be considered as:

- High when the voltage at the input terminal > V_{IT+}
- Low when the voltage at the input terminal < V_{IT-}

Figure 5.8: Threshold level for TOP IN and BOT IN



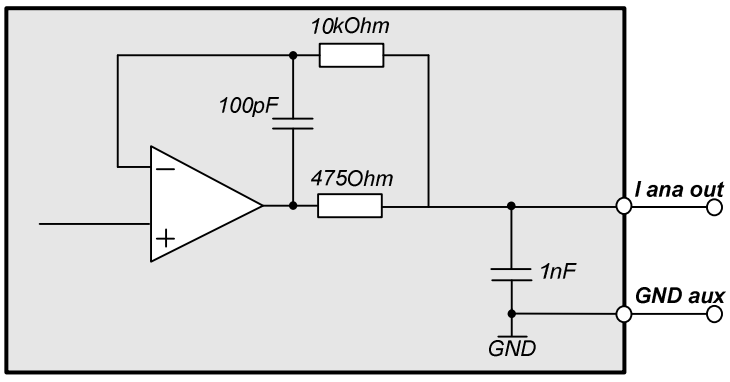
The threshold values V_{IT+} and V_{IT-} are given in the SKiiP®3 V3 datasheet on page 2.
For V_{IT+} the value is given as minimum value that is *at least* necessary in order to switch on the IGBT.
For V_{IT-} the value is given as maximum value that should not be exceeded in order to switch off the IGBT.

5.2.5 Analogue Output Signals

The schematic in the Figure 5.9 shows the analogue output circuit of the SKiiP®3 V3 control PCB.
This circuit is used for:

- Measurement of AC-current
- Measurement of DC-link voltage
- Measurement of DCB-sensor temperature

Figure 5.9: Schematics analogue output signals



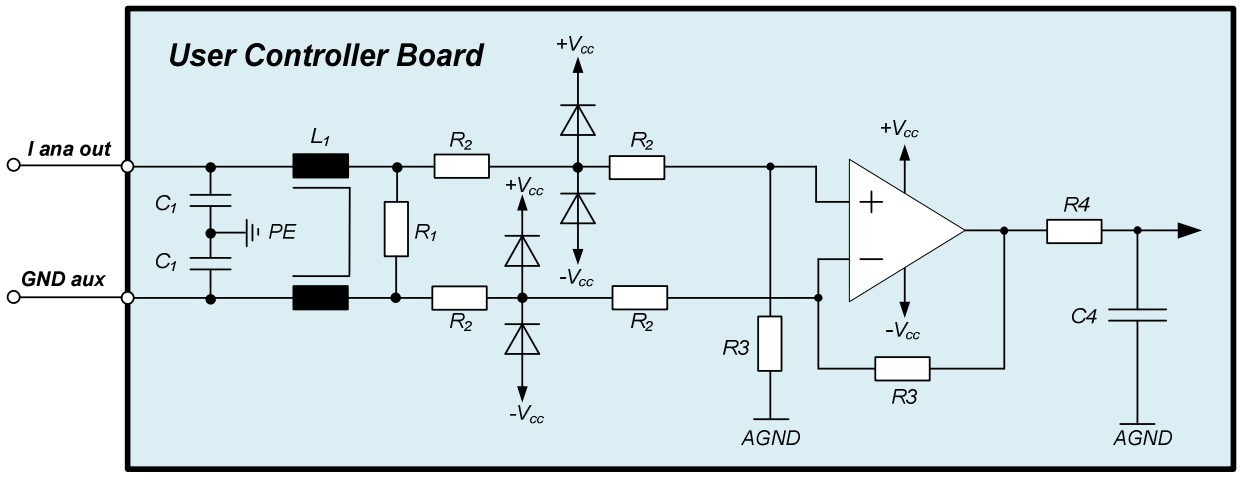
The 475Ω resistor in series with the voltage follower avoids damages caused by a temporary short circuit at the analogue output.

Please ensure that the maximum driven current by the output operational amplifier does not exceed 5mA.

A 1nF capacitor is used on the outputs to obtain high noise immunity.
On the user controller board a differential amplifier should be used which is connected to the analogue output and the corresponding ground signal “GND aux”. This ensures an accurate measurement of the analogue signals because this GND aux terminal is not used for supply currents and, hence, no voltage drop due to supply current will be caused.

A description for an equivalent analogue input circuit on the user controller board is given in Figure 5.10.

Figure 5.10: Application Example – Symmetric Wired differential Amplifier. Terminal description of pins *I ana out* and *GND aux* for current measurement



The recommended values below have to be checked in the application.

- The input capacitance C1 should not be higher than 1nF for current measurement and 10nF for temperature and voltage measurement to achieve stable operation of the amplifier circuit on the SKiiP®3 V3 board. Its signal response has to be checked in combination with the used signal cable.
- C1 leaks differential and common mode high-frequency interference currents. This capacitor reduces the bandwidth of the analogue signal. This can lead to control problems like AC current harmonics. Depending on the application PE should be connected to an appropriate ground, e.g. chassis ground.
- Resistor (R1). The interference sensitivity of the overall circuit (user control, driver) is reduced by a continuous current flow through this resistor. Recommended value: 10kOhm

Please note: Capacitors should not be used in parallel to the feedback resistor (R3) and also to the resistor of the non-inverting input to ground (R3). These capacitors have often high tolerances, so the common-mode rejection of the circuitry is reduced by this effect. No capacitor should be connected between the plus- and the minus-pin of the operational amplifier as well. This additional cut off frequency can lead to an oscillating signal.

- The input resistor (R2) should be split and installed between the clamping-diodes. The current through the diodes is limited by this resistor. A diode with a low reverse current should be selected e.g. BAV99.
- To achieve a good noise performance a low-impedance feedback-resistor should be used (R3). The value for the resistor must be chosen depending on the required gain factor.
- A low pass filtering stage should be implemented to avoid remaining differential interferences. It can be realised by a simple R-C network (R4, C4) at the end of an operational amplifier. The cut-off frequency of the filter should be adjusted with the behaviour of the operational amplifier used and the necessary bandwidth of the analogue signal (Temp/DC-Link/Current).
- A Rail-to-Rail amplifier is recommended for better performance. If a Rail-to-Rail amplifier is not applicable, the pin $-V_{CC}$ must be connected to the negative voltage instead of ground in order to use the complete voltage range of the amplifier especially close to 0V. The possible negative output voltage of the amplifier has to be considered by designing the following circuit.
- AGND should be connected to the ground of the analogue signal processing at the user controller board.

5.2.6 Error output

Characteristics and functionality:

- shows the status of the gate driver: enabled/disabled
- high active: HIGH = IGBT driver disabled, LOW = IGBT driver enabled (wire break monitoring)
- open collector output

The driver will turn off the open collector transistor to set the ERROR out signal to HIGH state over the pull-up resistor R_{pull_up} by following errors:

- Undervoltage at low voltage side of the driver board (refer to chapter 5.3.6.1)
- Undervoltage at high voltage side of the driver board (refer to chapter 5.3.6.1)
- SKiiP internal short circuit of DC+ and DC- (refer to chapter 5.3.6.2)
- OCP Protection (refer to chapter 5.3.7.1)
- Exceeding the maximum DCB temperature (refer to chapter 5.3.7.2)
- DC-link overvoltage (refer to chapter 0)

For information about failure management and error processing please refer to chapter 5.3.6, p.29.

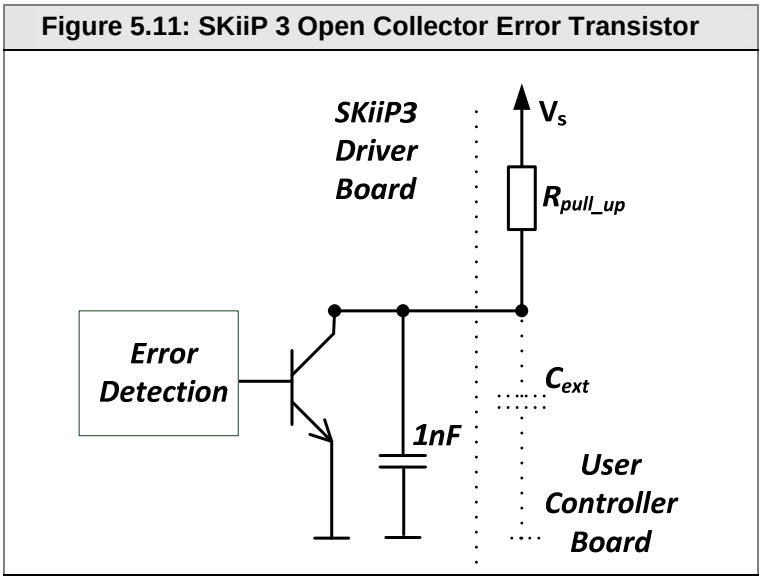
The error output of SKiiP®3 V3 is short circuit proof. All logical error outputs are open collector transistors with V_s=3,3-30V and I_{max}=15mA (see Figure 5.11). The external pull-up voltage should be set as high as possible but not higher than V_S. An external pull-up resistor to the controller logic high level in the range of $V_s/I_{max} < R_{pull\_up} < 10kOhm$ is required.

EXAMPLE: for V_s=15V the resistor should be in the range $(15V/15mA) < R_{pull\_up} < 10kOhm$, that is

$1kOhm < R_{pull\_up} < 10kOhm$.

The external filter's capacitor C_{ext} is not compulsory but is recommended to improve the noise immunity. The value in the range of a few Nanofarads (nF) should be chosen, because the RC-time constant must not exceed the minimum error memory reset time t_{pRESET} (given in the SKiiP®3 V3 data sheets, page 2).

Figure 5.11: SKiiP 3 Open Collector Error Transistor



5.2.7 Ground connection

SKiiP®3 V3 employs a power ground and an analogue ground. The power ground is used for power supply and reference of digital signals. The analogue ground is used to accurately measure of all analogue signals. All grounds are physically connected to each other on the gate driver board.
The analogue ground should be used as reference for differential amplifier inputs on the controller board to ensure accurate measurement (refer to Table 5-4).

Table 5-4: Ground connections of SKiiP®3 V3

Function	Signal
Power ground and digital grounds	GND
Analogue ground	GND aux

For the GD-Type SKiiP3 it is recommended:

- do not use one analogue ground for more than 2 analogue signals
- always use the nearest analogue ground

5.2.8 Shield and protective earth/chassis connection

The shield pin 1 of the DIN41651 connector is connected to GND at the Gate Driver board. At the Gate Driver board there is neither connection to heat sink nor other protective earth connections. On the user controller board the shield should be connected to chassis which is protective earth in isolation class 1 systems. This single ended grounding is effective against capacitive coupling e.g. from neighbouring conductors since the grounded shield forms the opposite pole of the parasitic capacitance. The interference current flows away via the shield. The GND of the user controller board can be connected to protective earth/chassis either directly or via a capacitor. This connection should be low inductive (e.g. metal bolts from PCB to chassis) and located close to the DIN41651 connector. Furthermore each signal output and input should have a capacitor linked to chassis. These measures will allow to bypass burst signals.

Figure 5.12: Ground and shield connection. Principle schematics for switching signal inputs

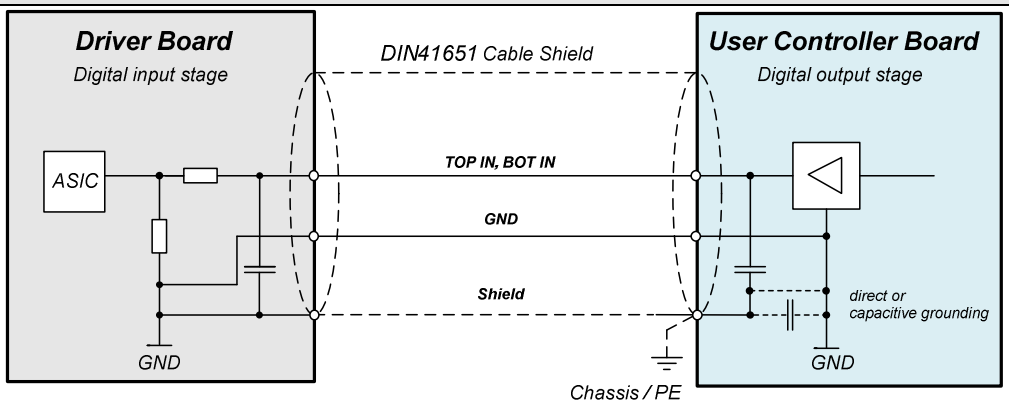
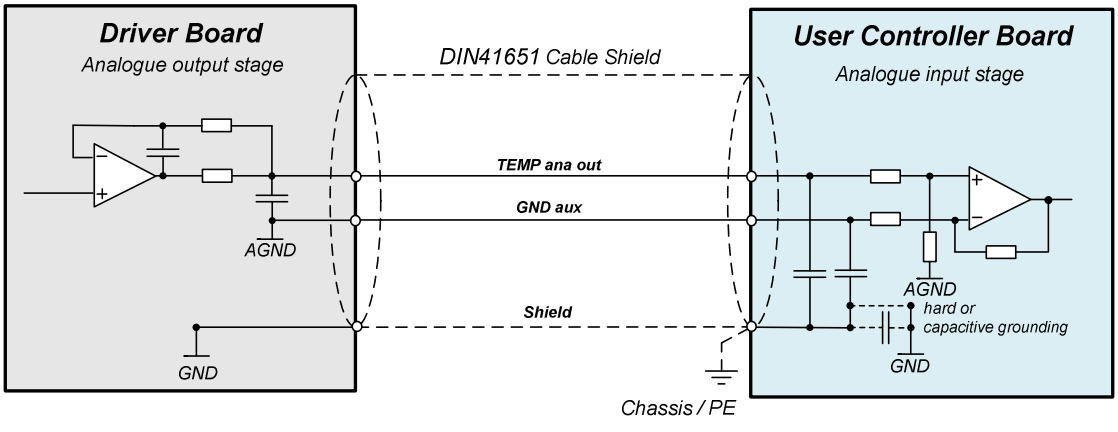


Figure 5.13: Ground and shield connection. Principle schematics for analogue output signal (Example: Temperature output)



5.3 Gate driver board

5.3.1 Overview

The SKiiP®3 V3 gate driver board includes following functions:

- Transferring digital input signals into powerful output signals to control the IGBT
- Power-on Reset (refer to chapter 5.3.2)
- Dead time generation (refer to chapter 5.3.3)
- Short pulse suppression (refer to chapter 5.3.4)
- Failure management (refer to chapter 5.3.6)

The gate voltages are provided as +15V for turn on and -8V for turn off.

5.3.2 Power-On-Reset

The Power-On-Reset is completed after the supply voltage will reach the level of 13V. It could take up to 150ms, this time is defined as t_{POR}.

Please note: After open collector transistor of error output will be reset (typ. 8ms) no error will be signalized during the remaining time of power on reset.To assure a high level of system safety the high and low side signal inputs should stay in a defined state (OFF state) during driver turn-on time. Only after the end of the power on reset, the IGBT operation is permitted.

5.3.3 Interlock Dead Time Generation

The interlock dead time is defined as t_{TD} in the SKiiP®3 V3 data sheet, page 2.
The dead time circuit prevents that high and low side IGBT of one half bridge can be switched on at the same time. The internal interlock time is adapted to the power semiconductors, i.e. is chosen as small as possible to allow high duty cycle but guarantees a safety margin against shoot through losses due to tail currents.
It is allowed to control the SKiiP®3 V3 by inverted pulses that means without controller side generated dead time. t_{TD} is not added to a dead time given by the controller. Additionally the switching on/off time of the IGBT $t_{d(on/off)IO}$ given in the data sheet SKiiP®3 V3, page 3, has to be taken into account (see Figure 5.14).

Please note: In case both channel inputs TOP IN and BOT IN are at HIGH level, the driver outputs V_{GETOP} and V_{GEBOT} will be turned off, but no error signal will be generated (see Figure 5.15).

5.3.4 Short pulse suppression

The short pulse suppression time is defined as t_{SIS} in the SKiiP®3 V3 data sheet.
This function suppresses short turn-on and off pulses at the pins TOP IN and BOT IN of the DIN41651 interface. In this way the IGBT chips are protected against spurious noise which can occur due to bursts on signal lines. Since the turn-on pulse is detected on one of the channels, the time counter starts which measures the duration of the pulse. If the overlaping is shorter than t_{SIS} the pulse will be suppressed, the other chanel remains on. No error will be indicated. The short pulse suppression time is included in the driver switch on/off delay time $t_{d(on/off)IO}$ given in the data sheet SKiiP®3 V3, page 3 (see Figure 5.14).

Please note: Noise pulses longer than t_{SIS} generate additional switching losses (min. on-time of the diode is > 3 µs) and must be considered during the junction temperature calculation in case of operation in harsh EMI environment.

Figure 5.14: Short pulse suppression, $t_{pulse}<t_{sis}$

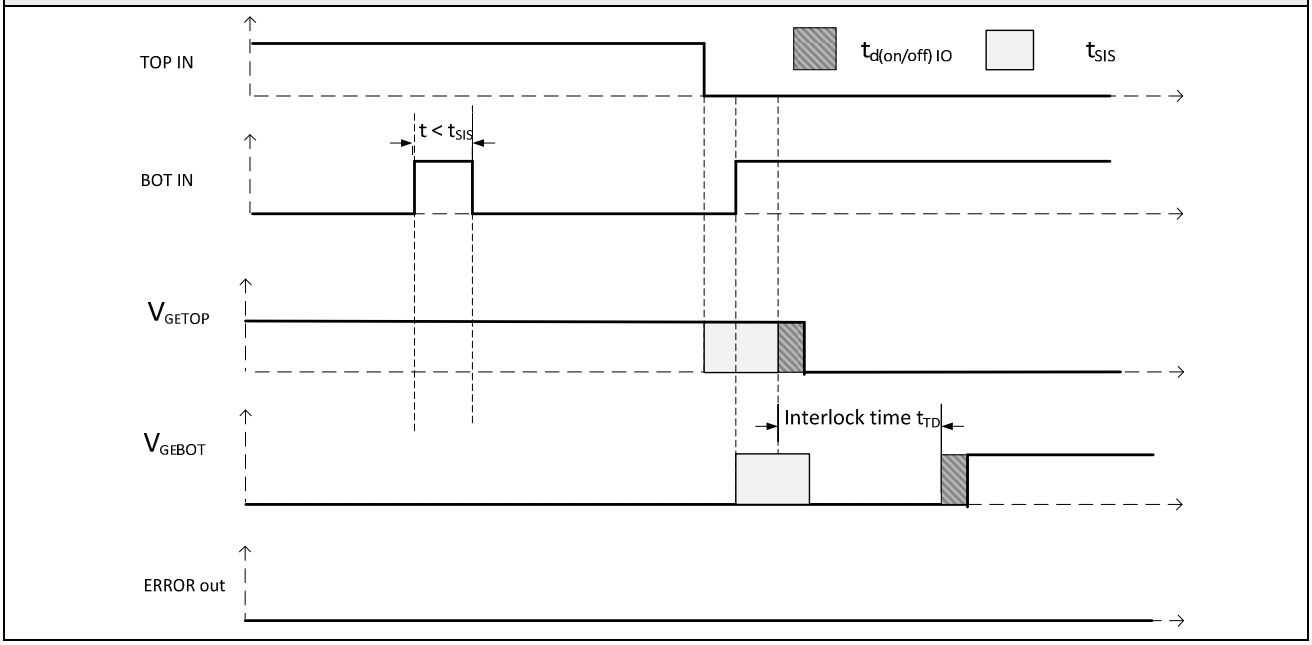
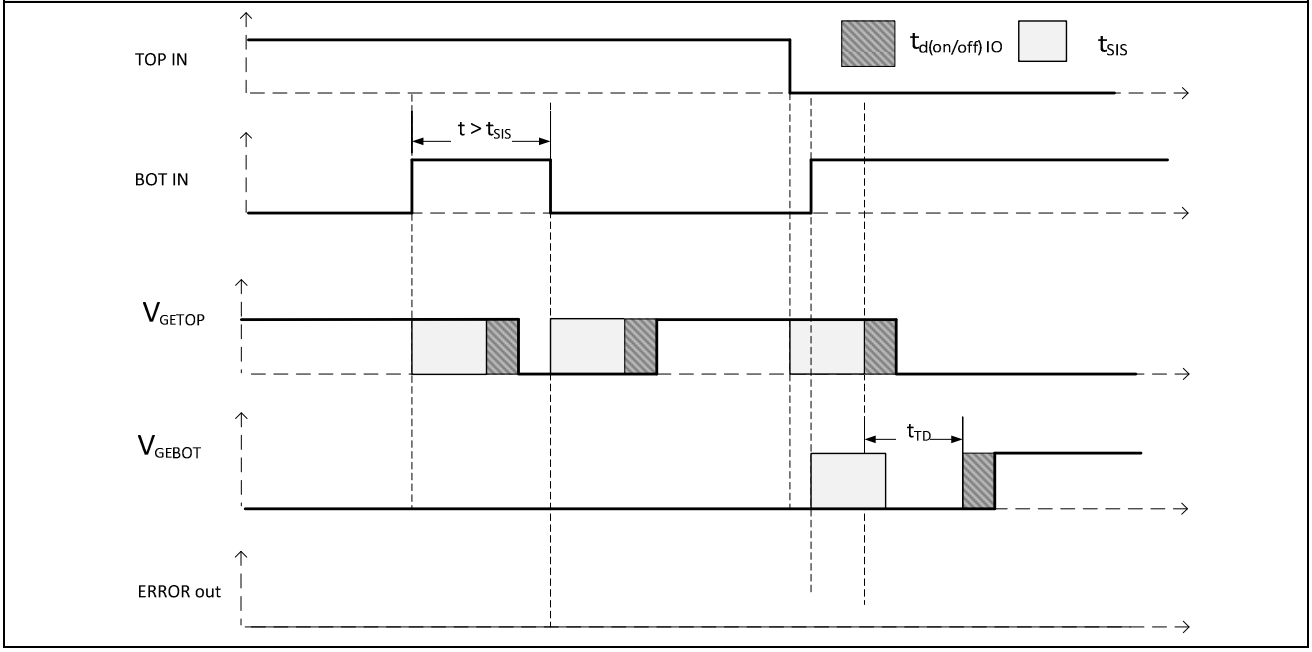


Figure 5.15: Short pulse suppression, $t_{pulse}>t_{sis}$



5.3.5 Switching frequency rating

The maximal possible switching frequency for SKiiP®3 V3 is given in the data sheet on page 1. No error signal will be set if the maximal allowed switching frequency for the particular SKiiP®3 V3 will be exceeded. It is the user's responsbility to limit the frequency according to the data sheet given maximum ratings.
The ambient temperature has got an influence on the max. possible switching frequency of SKiiP®3 V3, too. In case of higher ambient temperature the derating of the switching frequency must be considered (for all SKiiP®3 V3 types except of 4-fold GB-type). The derating diagrams for 2-fold and 3-fold GB-types as well as GD-type are shown in the Figure 5.16, Figure 5.17 and Figure 5.18 correspondingly.

Please note: Exceeding the max value ratings of the switching frequency provided in the corresponding SKiiP®3 V3 data sheet can lead to a damage of the SKiiP system and will result in loss of warranty in case of product claim.

Figure 5.16: Derating diagram for 2-fold GB-Type SKiiP®3 V3

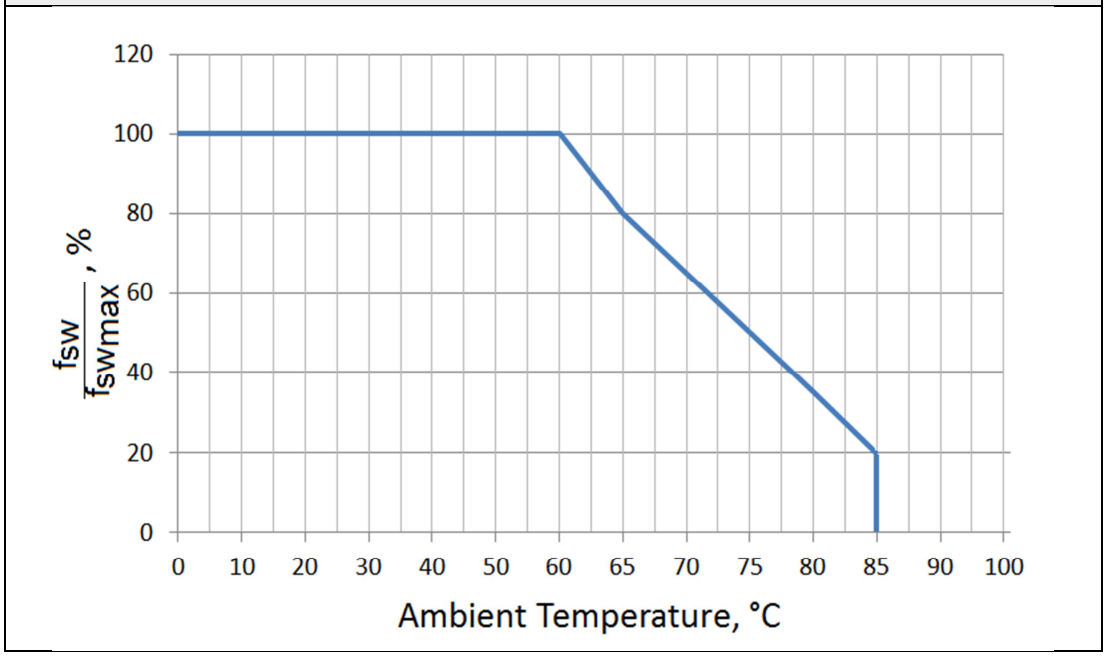


Figure 5.17: Derating diagram for 3-fold GB-Type SKiiP®3 V3

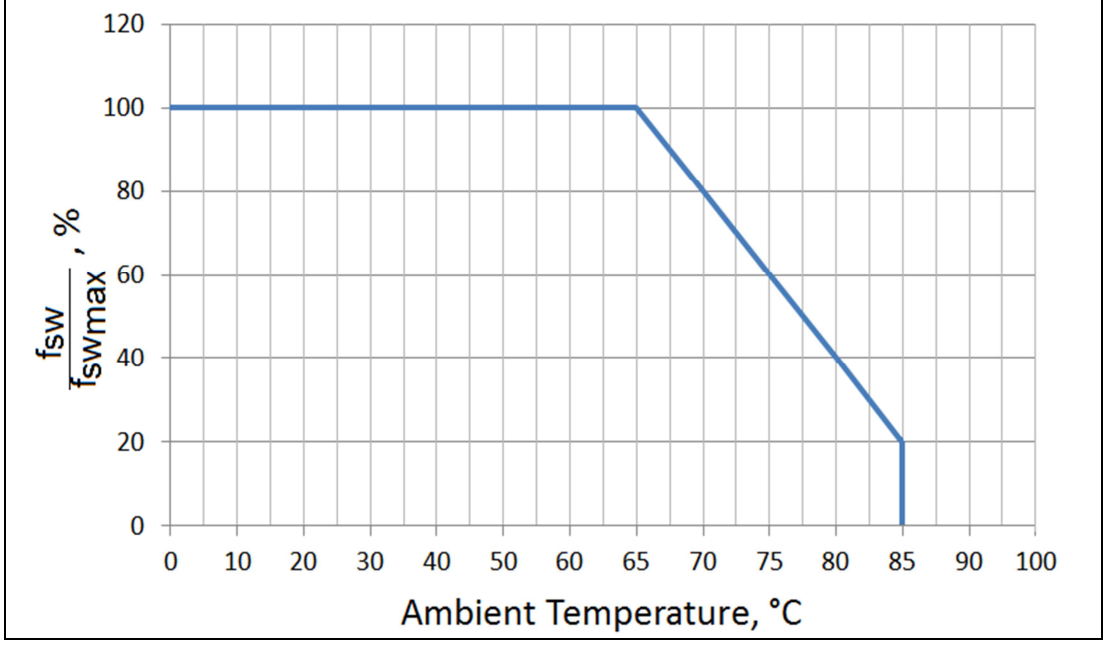
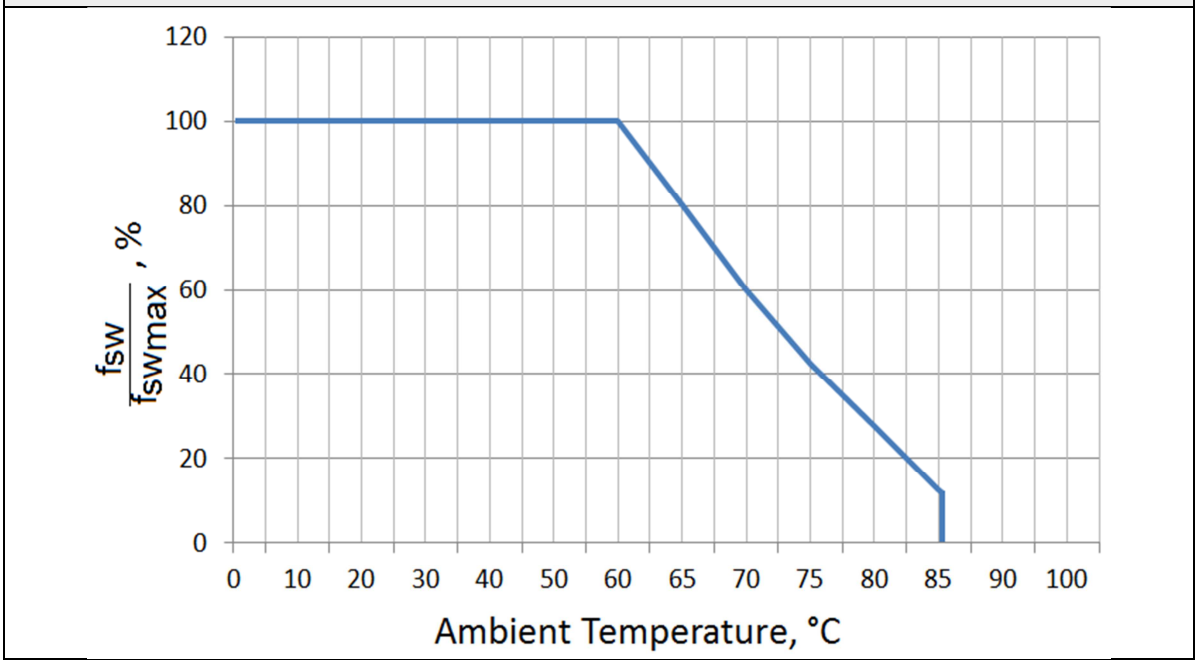


Figure 5.18: Derating diagram for GD-Type SKiiP®3 V3



5.3.6 Error Management

In case of an error caused by

- Undervoltage of the primary side (refer to chapter 5.3.6.1)
- Undervoltage of the secondary side (refer to chapter 5.3.6.1)
- SKiiP internal Short Circuit (refer to chapter 5.3.6.2)
- Overcurrent protection error (refer to chapter 5.3.7.1)
- Exceeding the maximum DCB-sensor temperature (refer to chapter 5.3.7.2)
- DC-link overvoltage (refer to chapter 0)

the driver will turn off the open collector transistor to set the ERROR out signal on the corresponding pins (see Table 5-5 for GB-type and Table 5-6 for GD-type SKiiP®3 V3) to HIGH state (not ready to operate) for the time error is present + at least error memory reset time. The IGBTs will be switched off and switching pulses from the controller won´t be transferred to the output stage. If the error is not present anymore the driver will check if the switching input signals TOP IN and BOT IN are both set to LOW for the t_{pRESET} time (refer to SKiiP®3 V3 data sheet, page 2). If this is the case the driver will release the ERROR out signal. If both input signals have not been switched to LOW state during the t_{pRESET} the driver will hold the open collector transistor turned off (to set the ERROR out signal to HIGH) as long as the switching input signals TOP IN and BOT IN are not LOW for t_{pRESET} time (see Figure 5.19). So the switching input signals TOP IN and BOT IN should be set to LOW after error message from driver has come and should not be activated before the ERROR out signal is in LOW state again.

Figure 5.19: Processing of ERROR out signal

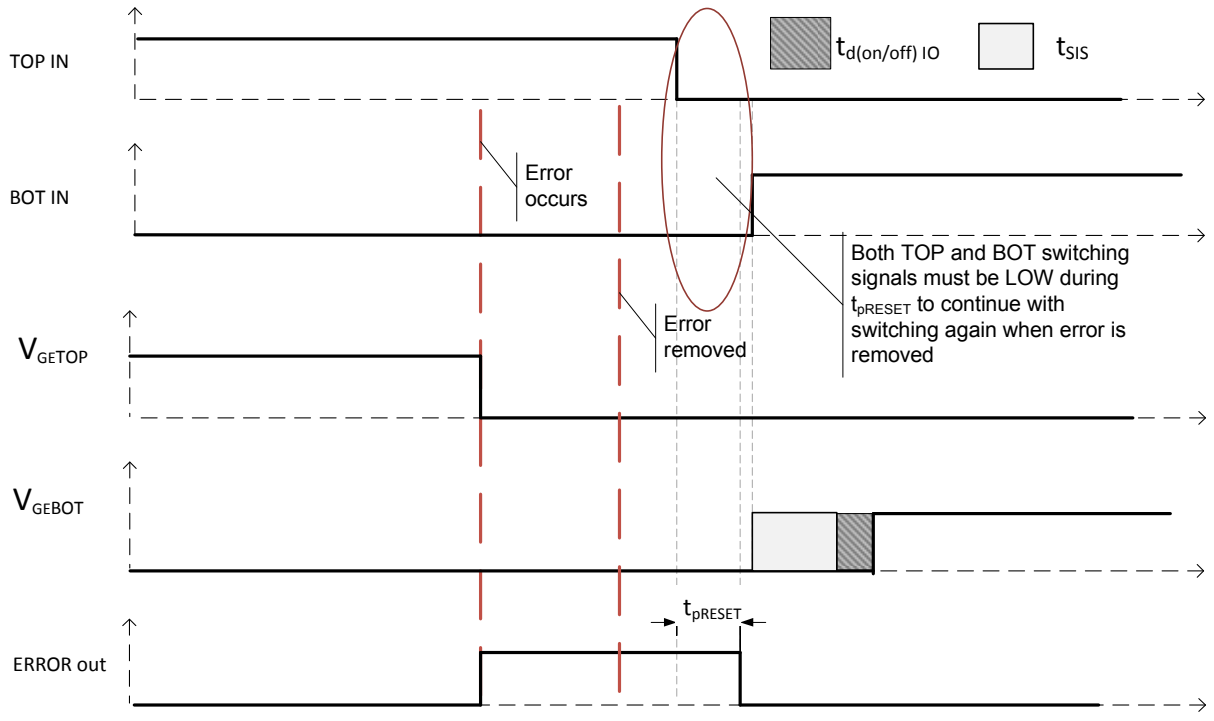


Table 5-5: Error management GB-type

	Pin 3: ERROR out	Pin 5: Overtemp. out
V_{CE}-Protection	x	
OCP-Protection	x	
Overtemperature protection	x	x
DC-Link overvoltage protection	x	
Internal supply voltages error	x	

Table 5-6: Error management GD-type				
	Pin 3: ERROR HB1 out	Pin 6: ERROR HB2 out	Pin 9: ERROR HB3 out	Pin 11: Overtemp. out
V_{CE}-Protection HB1	x			
V_{CE}-Protection HB2		x		
V_{CE}-Protection HB3			x	
OCP-Protection HB1	x	x	x	
OCP-Protection HB2	x	x	x	
OCP-Protection HB3	x	x	x	
Overtemperature protection	x	x	x	x
DC-Link overvoltage protection	x	x	x	
Internal supply voltages error	x	x	x	

5.3.6.1 Under Voltage Protection (UVP) supply voltage

The Gate Driver board is equipped with a UVP of the supply voltage which is based on the observation of the internal supply voltage level. The UVP of the low voltage side monitors the internal voltage 15V DC which is provided by the internal DC-DC converter (converts the unregulated input voltage to 15 V DC). Table 5-7 summarizes the trip level.

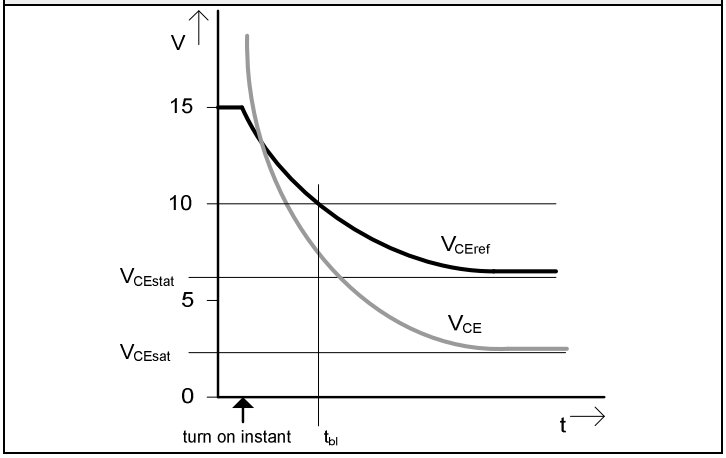
Table 5-7: Signal characteristics of Under Voltage Protection primary side	
Signal Characteristics	**typ. value**
Undervoltage protection trip level for internally regulated +15V	13,9V
Undervoltage protection trip level for internally regulated -15V	-13,9V
High voltage side protection level	10V

If the supply voltage of the driver board falls below the trip level, the IGBTs will be turned off (IGBT driving signals set to LOW). The switching input signals TOP IN and BOT IN will be ignored and the error signal ERROR out changes to HIGH state. The system restarts after the error memory reset time, if the supply voltage exceeds the threshold level and the TOP/BOT switching signals are LOW.

5.3.6.2 Dynamic Short Circuit Protection (DSCP)

The DSCP circuit is facilitating the short circuit sensing in case of internal short circuit (“shoot through” protection). It monitors the collector-emitter voltage V_{CE} of the IGBT during its on-state. Due to the direct measurement of V_{CEsat} on the IGBT's collector, the DSCP circuit switches off the IGBTs and an error is indicated if the V_{CEsat} is too high.

Figure 5.20: Reference voltage (V_{CEref}) characteristic



After t_{bl} is over, the V_{CE} monitoring will be triggered as soon as $V_{CE} > V_{CEref}$ and will turn off the IGBT. The switching input signals TOP IN and BOT IN will be ignored and the error signal ERROR out changes to HIGH state.

Figure 5.21: Turn on of IGBT too slow*

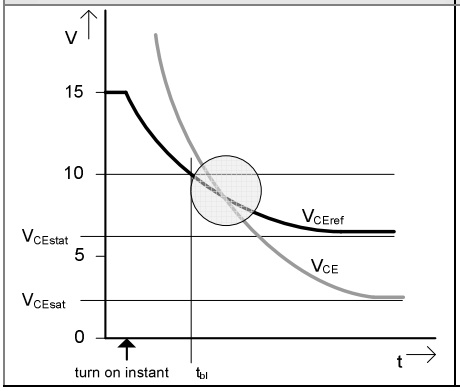


Figure 5.22: Short circuit during operation

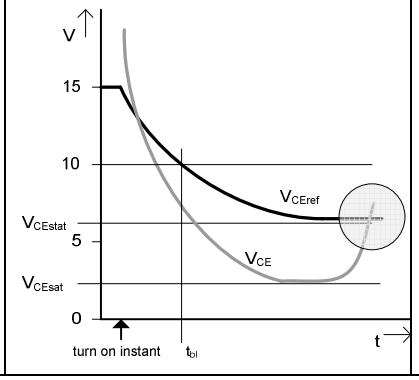
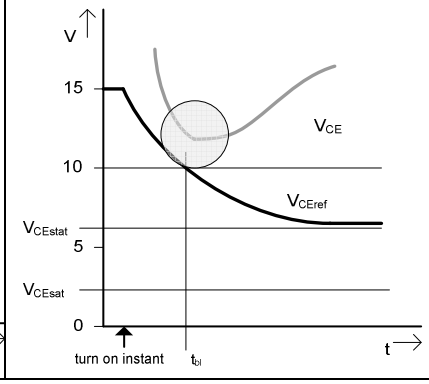


Figure 5.23: Short circuit during turn on



* or adjusted blanking time too short

5.3.7 Analogue signals / sensor functionality

5.3.7.1 AC-Current sensor

Each half bridge module (refer to Figure 2.1) integrates one AC-current sensor. The measured current is normalized to a corresponding voltage and is available at the DIN41651 interface with the characteristic given below:

Table 5-8: Signal characteristic of current measurement

Signal Characteristics per SKiiP®3 V3	Value
Analogue current trip level I_{TRIPSC} @ I ana out = 10V	Please see the corresponding data sheet SKiiP®3 V3, page 2
Small signal bandwidth, $f0_{Iana}$	50 kHz
Signal Offset for low currents[1)]	± 5mV

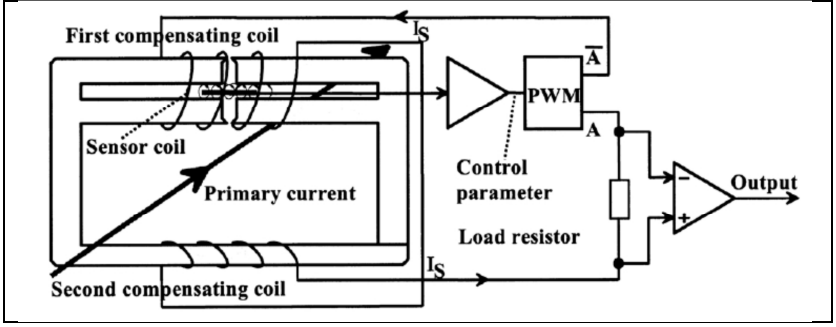
The current sensor signal could be used for AC current control. Moreover these sensors are used to protect the SKiiP against over current. The over current protection reacts independently from the temperature level and provides a reliable protection of the SKiiP system. If the AC output current is higher than I_{TRIPSC} (please see corresponding data sheet SKiiP®3 V3 page 2 for the exact value), the IGBTs are immediately switched off and switching pulses from controller are ignored. The error signal ERROR out will be set to HIGH state.
In all SKiiP®3 V3 with Al_2O_3 ceramic substrate 100% of the rated DC current I_C corresponds to 8V and the over current trip level I_{TRIPSC} is set to 125% I_C, equivalent to 10V.
SKiiP®3 V3 systems with AlN ceramic substrate are from the electrical point of view similar to the same sized Al_2O_3 substrate based systems but have a better thermal conductivity and therefore a higher rated DC-current. As there is no difference of the driver boards for AlN and Al_2O_3 DCB regarding current normalization, over current trip level etc., both the Al_2O_3 substrate based systems have the same relation between the absolute values of current and the corresponding voltage. Only the relation in percent to I_c is different (please see corresponding data sheet SKiiP®3 V3 page 2 for an exact value).

Please note: Over current protection cannot protect the diodes from overload, because the diode current cannot be turned off. Please use suitable fuses to protect the diodes.

Current sensor operation principle

The current transformers work according to the compensation principle. The magnetic field caused by the load current is detected by a magnetic field sensor. This is not a Hall element but a small coil with a highly permeable core. Due to the properties of this sensing element there is low gain and linearity error. An electronic circuit evaluates the value of the field sensor and feeds a current into the compensation coil thus keeping the effective magnetic field to zero. The compensation current is acquired across the voltage drop of a burden resistor with an electronic circuit and provides an image of the actual load current. The SKiiP®3 V3 current sensor uses a digital controller to generate the compensation current while an analogue controller has been used in the SKiiP®2 design. Figure 5.24 illustrates the compensation principle with the current sensor employed in the SKiiP®3 V3.

Figure 5.24: Compensation principle of SKiiP®3 V3 current sensor



The Table 5-9 provides an overview of the SKiiP®3 V3 current sensor's basic data:

Table 5-9: Characteristics of the SKiiP®3 V3 current sensor

Parameter	SKiiP®3 V3
Continuous output current per current sensor	400 A_{rms}
Short time output current, 2 s per current sensor	500 A_{rms}
Peak current, 10 µs	3000 A
Parasitic capasitance prim. – sec. per current sensor	30 pF

The accuracy of the current sensor depends on several points as there are:

- tolerance of the current sensor
- tolerance of the burden resistor of the current sensor
- tolerance of SKiiP®3 V3 internal amplification circuitry (e.g. by offset of operational amplifiers, tolerances of external passive components etc.)
- tolerance due to temperature drift

The maximum tolerance values can be calculated by the following equation[1)]:

$\Delta I = I_C$ * 0,13% + I_{actual} (1,37% + |ΔT| * 0,002%/K), where:

- ΔI is the absolute deviation of the current value per half bridge
- Ic is the nominal current per half bridge
- I_{actual} is the actual measured current level per half bridge
- ΔT is the difference between T_{amb} and 25°C

Example: For a SKiiP®3 V3 GD-Type (SKiiP513GD172 with Ic = 500A) the deviation at the current level of I_{actual} =300A and T_{amb}=85°C:

ΔI = 500A *0,13% +300A* (1,37% + I 85°C-25°C I*0,002%/°C) = 5,12A

1) By calculation of the accuracy for low currents the offset value from Table 5-8 cannot be neglected and has to be considered as additional tolerance.

5.3.7.2 Integrated DCB-temperature sensor

The integrated DCB-temperature sensor is a chip resistor with PTC characteristic. The sensor is soldered onto the ceramic substrate close to the IGBT and freewheeling diode chips and is isolated. An evaluation circuit realized on the integrated driver provides a normalized, analogue voltage signal of the actual ceramic substrate temperature value (see **Fehler! Verweisquelle konnte nicht gefunden werden.**). The analogue temperature signal is available at the DIN41651 interface with the characteristic given below:

Table 5-10: Characteristics of the DCB-temperature sensor circuit

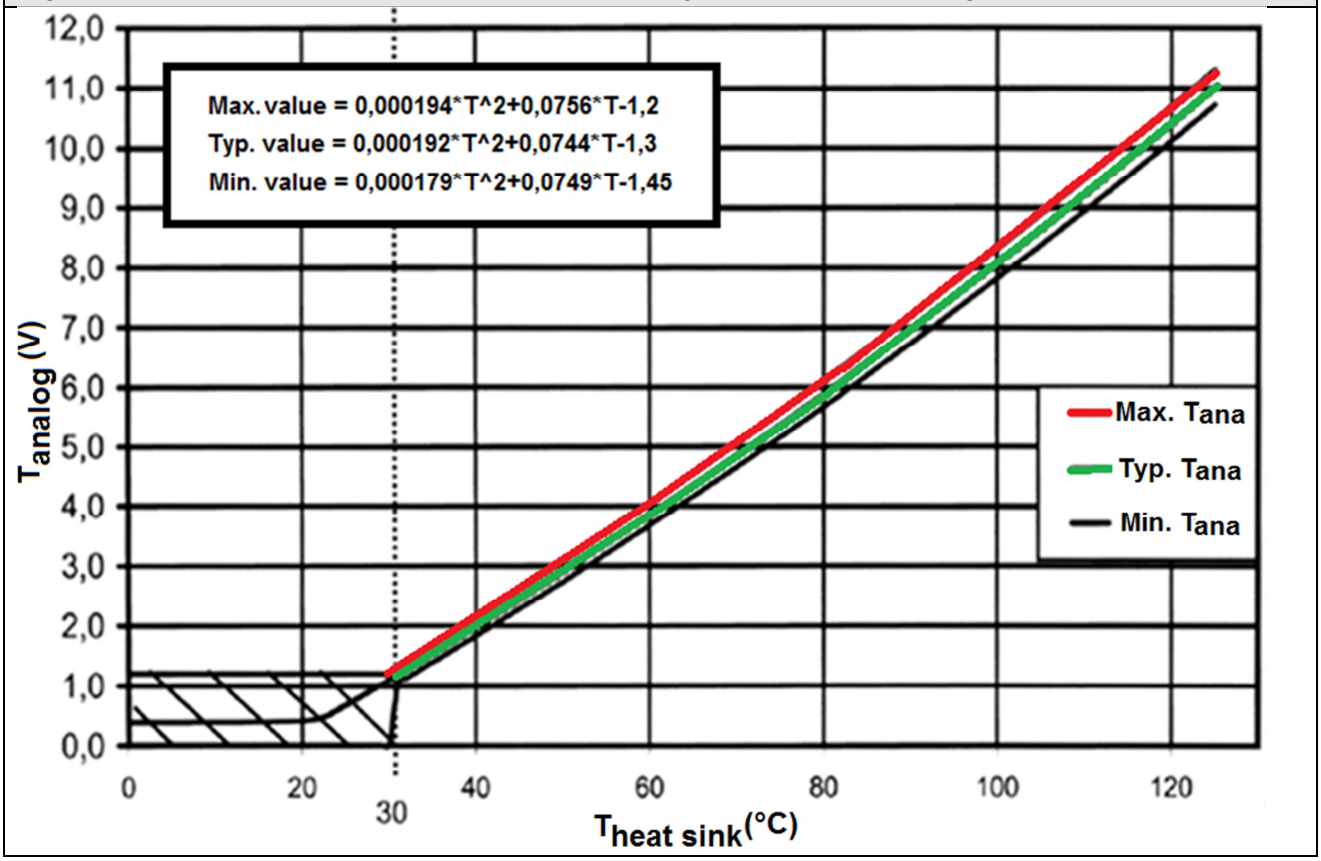
Temperature signal characteristics	Value
Trip level T_{trip}	115°C
Minimum measurable temperature T_{MIN}	+30°C
Analogue temperature signal TEMP ana out @ 115°C	10V
Analogue temperature signal TEMP ana out @ 30°C	1V
Accuracy of analogue signal @ T_{trip}	±3%
Bandwidth, f_{0Tana}	5Hz

Please note: The temperature sensor is designed for T_r > 30°C, because the tolerance band is too wide for temperatures below 30°C.

If the signal $Temp_{ana}$ out from temperature sensor reaches the trip level, the IGBT are switched off and switching pulses from controller are ignored. The error signals ERROR out and Overtemp out will be set in HIGH state. The ceramic substrate temperature is very close to the heat sink temperature. The trip level of 115°C is sufficient for most air cooled applications to protect the system, but for water cooled systems or short time overloads the threshold might be too high. In this case another protection trip level is needed and the customer can use the analogue temperature output to protect the system.
In general for both air- or water cooled systems the protection of the built-in temperature cannot perfectly protect the SKiiP against over temperature, especially when sufficiently fast transient load conditions occur. A detailed system verification is required to verify the efficient protection under customer specific conditions.

Please note: The ceramic substrate temperature is very close to the heat sink temperature, therefore it can be used to check the SEMISEL calculation: if the DCB-temperature value coming from SKiiP®3 V3 during the real operation is close to the heat sink temperature given in the results of SEMISEL calculation, then for a steady state operation the calculated chip temperature is ideally also very close to the real chip temperature.

Figure 5.25: Characteristic between DCB-sensor temperature and the voltage at TEMP ana out



5.3.7.3 DC-Link-Voltage Sensing

Please note: The DC-link-voltage sensing is available for all GD-type SKiiP®3 V3. For GB-type SKiiP®3 V3 the DC-link-voltage sensing is available only on request instead of temperature measurement.

The DC-link-voltage (V_{DC}) is sensed at DC plus and DC minus terminal by means of internal serial resistor divider and a high impedance differential amplifier. The circuit is designed, manufactured and tested for safety isolation according to the standard EN50178. The normalized analogue DC-link voltage signal is available at the DIN41651 interface with the characteristic given in Table 5-11. The analogue output signal U_{DC} ana out is filtered with a time constant of 500µs.

Table 5-11: V_{DC} characteristics

V_{DC} signal characteristics	**1200V System**	**1700V System**
Analogue DC-link voltage signal U_{DC} ana out @ 900 V	9V	6,5V
Analogue DC-link voltage signal U_{DC} ana out @ 1170 V		9V
Accuracy of analogue signal @ V_{DCtrip} over full temperature range	±2,5%	
Bandwidth, f_{0Uana}	320Hz	

The DC-Link overvoltage protection is implemented for GD-types SKiiP®3 V3 and optionally for some customized GB-types. In case the DC-Link overvoltage protection is implemented and the operating DC-Link voltage is higher than V_{DCtrip} given in the corresponding data sheet SKiiP®3 V3 page 2, the IGBTs will be immediately switched off and switching pulses from controller will be ignored. The error signal ERROR out will be set in HIGH state.

6. Power terminals

6.1 Electrical limits

The power terminals have been designed to carry a certain rms current while providing sufficiently low electrical loss. Hence, a feasible rms current level is specified in the corresponding datasheet. Please refer to the corresponding section of the SKiiP module.

6.2 Mechanical constraints

6.2.1 Torque for terminal connection

The nuts contained in the plastic housing are utilized to ensure a proper pressure between the external connections and the terminal of the SKiiP. The applied torque to the screw shall be sufficient to ensure such safe connection to the terminals but should not exceed a specified torque to limit the mechanical stress to the plastic housing preventing any damage of the plastic body. Please refer to the corresponding information contained in the datasheet to adjust the mounting tool accordingly.

6.2.2 Static stress to the power connections

The power terminals of the SKiiP®3 V3 are robust against external forces which may be caused by the connection of the DC-link and load cables. Nevertheless, the SKiiP module is NOT MEANT to support the DC link. A separate mechanical support must also be provided for the AC connection (e.g. inductor or motor cables) in order to protect the power terminals from mechanical forces and vibration stress. The maximum forces that must not be exceeded are given in Table 6-1.

Table 6-1: Maximum allowed forces to terminals

Force	Maximum allowed force [N]
F_{+x}/ F_{-x}	<100
F_{+y}/ F_{-y}	<100
F_{+z}	<100
F_{-z}	<200

The following should be considered in the design process:

- DC connection:
  - Mechanical tolerances, especially when larger DC-links are used which are connected on more than one SKiiP
- Thermal expansion:
  - The DC-link is heated up under load and expands. This causes mechanical forces on the terminals.
- Stiffness of terminals for DC connection:
  - The connections should be soft in order to minimize the mechanical forces. This can be realized e.g. by using of tempered copper.
- Terminal hole diameter:
  - Should be large enough that the screw fits through the hole into the SKiiP connection.
- Dimensions of the DC connections:
  - Considering the heating and isolation. The terminals must not heat up snubber capacitors.

Recommended AC connection:

- Symmetrical AC connections for symmetrical current sharing between the paralleled half bridge modules. The load cable should be connected in the middle of the AC terminal and have equal distance to the each half bridge module.
- Connect a plate (e.g. copper) on all AC terminals of one SKiiP
- Cables can be connected on the same plate but it has to make sure that the cables do not apply force on the terminals (pull or push). Therefore flexible cables with stress relief should be used.
- The plate should be fixed by fixing poles. These poles shall be mounted directly on to the heat sink or a fixed frame construction and placed close to the SKiiP device.

7. Application hints

7.1 Verification of the design

Measurements and calculations have to be carried out to be sure that the design works reliably. The following points have to be considered:

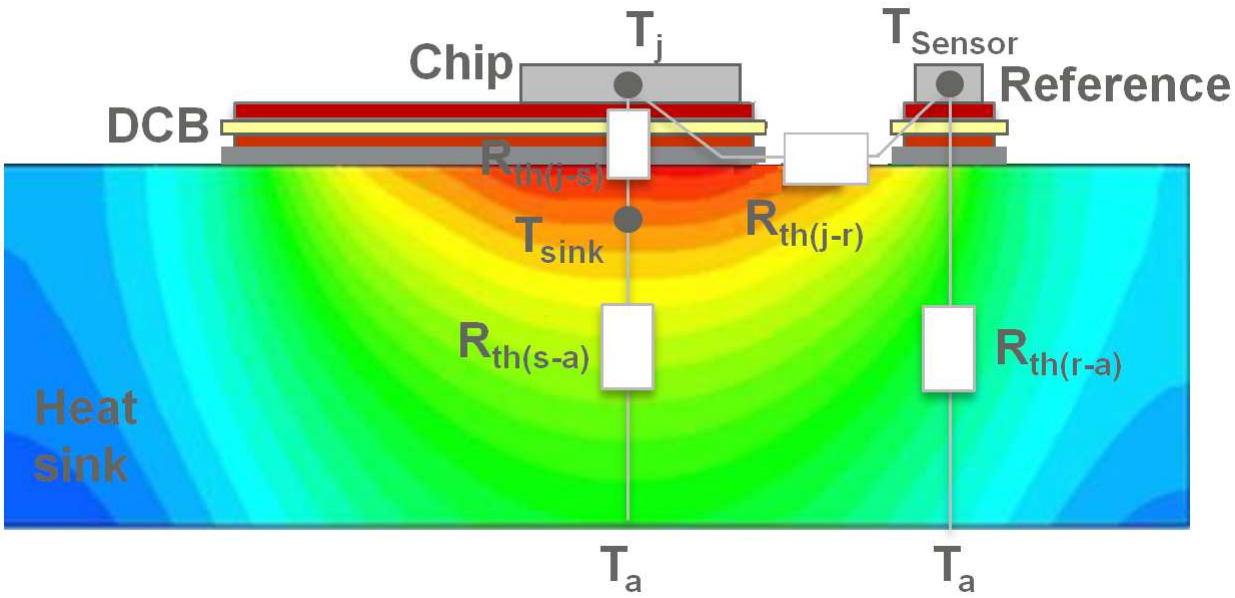
- Recommended IGBT and diode junction temperatures must not be exceeded also considering overload conditions
- Maximum blocking voltage V_{CES}/V_{RRM} must not be exceeded in any case (normal conditions, transient and short circuit)
- Load current of snubber capacitors
- Current sharing between paralleled half bridge modules
- Environmental temperature of driver board which affects the lifetime of the driver board electronics
- Load and temperature cycles which affect the lifetime of the power stage
- Environmental conditions during operation, transport and storage
- EMC design
- Mechanical design

Besides these general points application specific conditions and requirements need consideration, too.

7.2 Definition of Thermal Resistance

The definition of the thermal resistances given in the SKiiP®3 V3 datasheet are shown in Figure 7.1.

Figure 7.1: Definition of thermal resistances



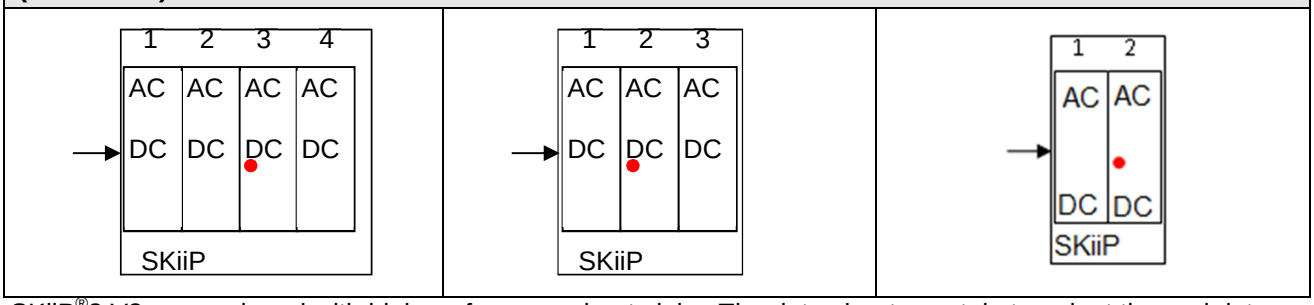
T_j	**junction temperature of the hottest chip**
T_{sensor}	**DCB-sensor temperature**
T_{sink}	**heat sink temperature in a drill hole 2mm underneath the chip**
T_a	**ambient temperature (coolant air or liquid)**
$R_{th(j-r)}$	**thermal resistance between junction and temperature sensor**
$R_{th(j-s)}$	**thermal resistance between junction and heat sink**
$R_{th(s-a)}$	**thermal resistance between heat sink and ambient (coolant air or liquid)**
$R_{th(r-a)}$	**thermal resistance between temperature sensor and ambient (coolant air or liquid)**
P_{losses}	**Power losses of the chip**

In general, the thermal resistance between two points 1 and 2 is defined according to following equation:

$$R_{th(1-2)} = \frac{\Delta T_{12}}{P_{losses}} = \frac{T_1 - T_2}{P_{losses}}$$

The data sheet values $R_{th(j-s)}$, $R_{th(r-a)}$ and $R_{th(j-r)}$ of the thermal resistance are calculated from experimentally measured data. The reference point of the temperature measurement has a major influence on the thermal resistance because of a temperature profile between the different chip positions and across the heatsink surface.
The reference points for SKiiP®3 V3 modules are: Virtual junction temperature of the hottest chip (T_j); heat sink temperature underneath the hottest chip (T_{sink}) and DCB-sensor temperature (T_{sensor}). A principle sketch with the positions is shown in Figure 7.1. The junction temperature Tj can be calculated by using the thermal resistors $R_{th(j-r)}$ and $R_{th(r-a)}$. SKiiP modules have no base plate, therefore the case temperature T_C can not be measured without disturbance of the thermal system and the thermal resistance $R_{th(j-c)}$ cannot be given.
To simplify the comparison to the other semiconductor modules SKiiP®3 V3 data sheets also contain the thermal resistance between chip junction and heat sink $R_{th(j-s)}$. T_{Sink} is measured in a drill hole 2mm underneath the heatsink surface. The 2 mm distance guaranties a low disturbance of the thermal path and a minimum effect of heat sink parameters like size, thermal conductivity, cooling medium etc.
The temperature sensor is located close to the DCB-edge on the separate DBC copper layer. This makes the temperature difference between junction and sensor higher and between sensor and ambient lower in comparison to SKiiP4.
Only one of the temperature sensors is monitored by the Gate driver. The monitored sensor is in the middle of the SKiiP (refer to Figure 7.2). The protection level is matched to the maximum operation temperature of the power semiconductors.
During operation there will be a temperature profile along the heatsink from cool at the inlet of the coolant to warm at the outlet.

Figure 7.2: Sensor position in SKiiP®3 GB- and GD-Type (2fold, 4fold, 3fold) with proposed cooling (water inlet) direction



SKiiP®3 V3 are equipped with high performance heat sinks. The data sheets contain transient thermal data referenced to the built-in temperature sensor. This allows the calculation of junction temperature Tj, if the generated losses are known. The thermal resistances given in the data sheets represent worst case values.
Evaluation of thermal impedance:

- Junction to sensor

$Z_{th(j-r)} = \Sigma R_{th(j-r)n} * (1-e^{-t/Tn})$, n=1,2,3,….

- Sensor to ambient
- $Z_{th(r-a)} = \Sigma R_{th(r-a)n} * (1-e^{-t/Tn})$, n=1,2,3,….

Please note: The values for the transient thermal impedance given in the data sheets ($Z_{th(j-r)}$) are only valid together with the SEMIKRON standard heat sinks and under conditions given in the data sheets. The usage of these values for other heat sinks/conditions might cause deviations in calculation of thermal resistance!

7.3 Cooling circuit and coolant

The cooling circuit (heat sink) of the water-cooled SKiiP®3 IPM consists of two side parts (with inlet and outlet for coolant marked on the corresponding data sheet) and the cooling channels inside the SKiiP cooling plate as well as turbulators. The heat sink cooling channels of each half-bridge of the internal IGBT power module are connected in serial. The cooling circuit contains following parts as shown in the table below:

Part of cooling circuit	Used material
heat sink plate	EN AW-6060 T66 (AlMgSi 0,5 F22) if nothing else is specified
side parts	EN AW-6060 T66 (AlMgSi 0,5 F22) if nothing else is specified
sealing gasket	EPDM 70 Shore A
turbulators	EN AW-5754 (AlMg3)

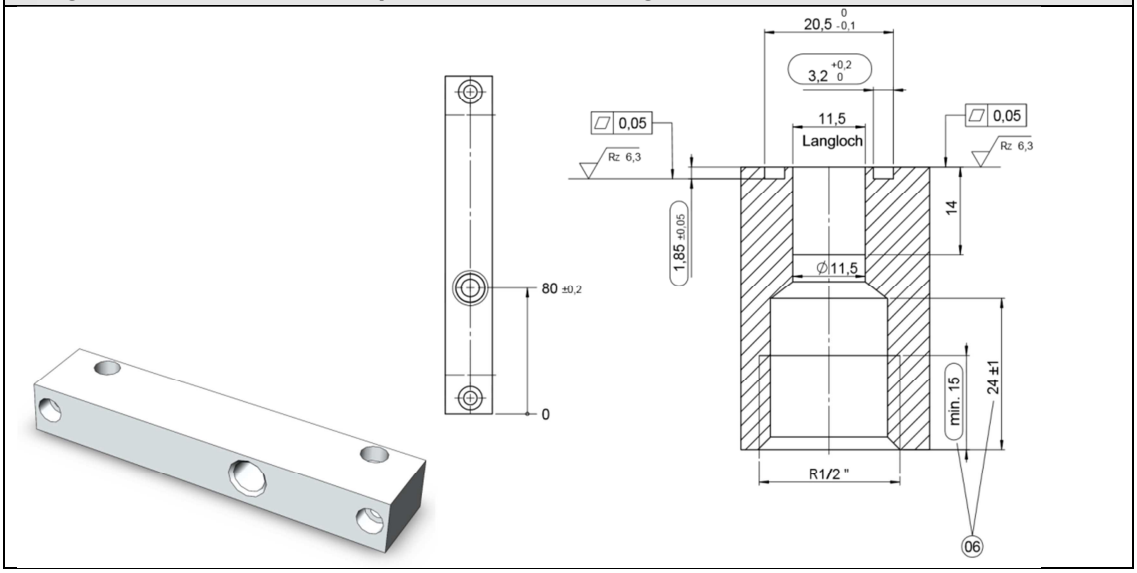
Regarding the selection of the coolant type the used materials of the cooling circuit need to be considered. The user has to ensure that the used coolant is compatible with the cooling circuit materials to avoid e.g. corrosion or freezing at low temperatures. SEMIKRON proposes the usage of a mixture of water and glycol with corrosion inhibitor. The percentage of glycol in the cooling medium shall be at least 10%. All thermal performance data given in the corresponding SKiiP®3 V3 data sheets assume a mixture of 50% water and 50% glycol if nothing else is specified.
For ongoing information and hints concerning cooling circuit / coolant please refer to SEMIKRON Application manual for Power Semiconductors [2].

7.4 Water connection description of water-cooled SKiiP®3

SKiiP®3 side cap:

- Thread R ½ (DIN 259) → correspond to G ½ (DIN EN ISO 228)
- Thread depth 15mm!

Figure 7.3: SKiiP®3 side cap mechanical drawing



Thread in side cap:

- Older drawings (before 2013) R ½ (DIN 259)
- Newer drawings (since 2013) G ½ (DIN EN ISO 228)

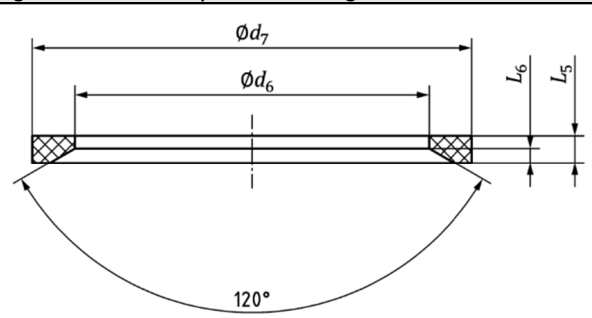
Recommended pipe fitting:

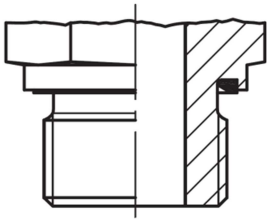
- Fitting ISO 1179-2 — G 1/2 A — L
- Fitting ISO 1179-3 — G 1/2 A — G

Fitting ISO 1179-2 — G 1/2 A — L

- Fitting of shape E according to ISO 1179-2 with G ½ thread, tolerance class A (DIN EN ISO 228), L is for „lower“ pressures (max. 250 bar)
- Sealing with a additional profile-sealing ring (rubber) according to ISO 1179-2 – G 1/2 A
- Dimension of profile-sealing ring according to ISO 1179-2:
  - D6 [mm]= 18,5
  - d7 [mm]= 23,9
  - L5 [mm]= 1,5
  - L6 [mm]= 0,8

Figure 7.4: Description of fitting ISO 1179-2 — G 1/2 A — L

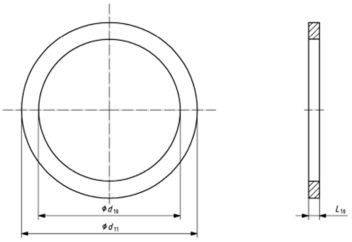


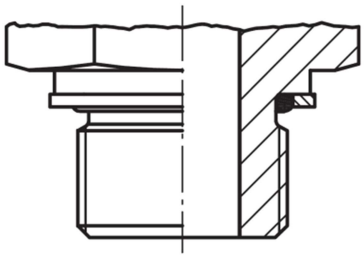


Fitting ISO 1179-3 — G 1/2 A — G

- Fitting of shape G according to ISO 1179-3 with G ½ thread, tolerance class A (DIN EN ISO 228), G is the type of the sealing
- Sealing (type G) with a additional O-ring, which is framed by a metal support ring
- Dimensions of metal support ring and O-Ring according to ISO 1179-3:
  - Stützring [mm]: d10 =23,3 | d11 = 28,5 | L10 = 1,9
  - O-Ring [mm]: d8 = 17,86 | d9 = 2,62

Figure 7.5: Description of fitting ISO 1179-3 — G 1/2 A — G





Fitting DIN 3852-2 — C — R ½ is not reccomended → only in exceptional case!

Please note: The given specifications for sealings of the pipe fittings are recommended values and have to be validated by customer depending on production equipment and application.

7.5 Maximum blocking voltage and snubber capacitors

The maximum blocking voltage V_{CES}/V_{RRM} which is given in the SKiiP®3 V3 datasheet must not be exceeded. It must also be considered that IGBT switches faster when the junction temperature is low. The first countermeasure to keep the overvoltage on the semiconductor low is a low inductive DC-link design. In addition, suitable snubber capacitors are recommended, which should be mounted directly on the DC-link terminals of each half bridge module. The application note AN-7006 “Peak voltage measurement and snubber capacitor specification” provides the information how to perform the tests and to select the snubber capacitors. The following snubber capacitors are recommended for SKiiP®3 V3. This recommendation is purely indicative - it has to be validated by testing that the capacitors are compatible with the design and will not be overloaded.

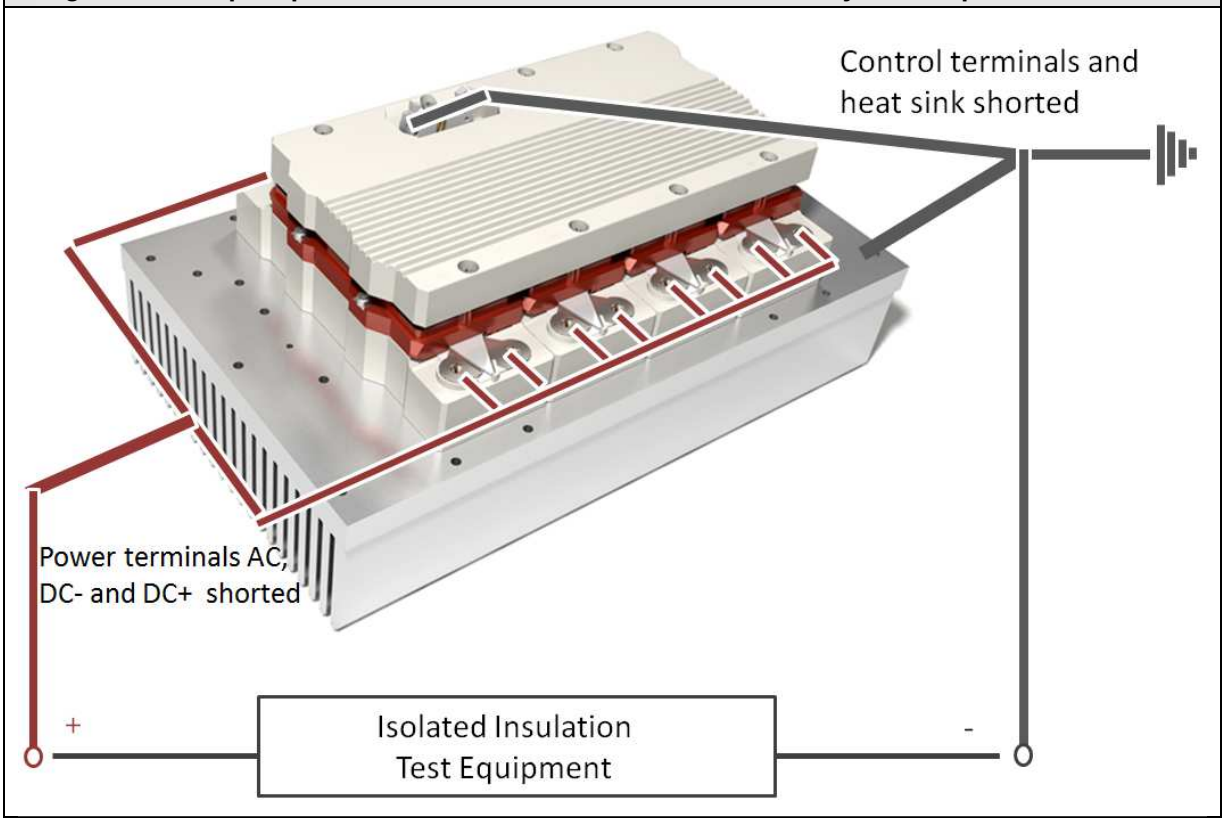
Table 7-1: Snubber capacitors for SKiiP®3 V3

Capacitance / DC voltage	For use with
470 nF / 1000V	1200V device
220 nF / 1250V	1700V device

7.6 Isolation voltage test (IVT)

During production test the isolation voltage of 5600Vdc (1700V devices) or 4300Vdc (1200V devices), DC, each polarity, is applied to 100% of the SKiiP-systems for 1s with a test set up shown in Figure 7.6 These values are also available in the corresponding datasheets.

Figure 7.6: Graphic presentation of the electrical connections by the IVT procedure



The polarity change (whereas the heat sink is always grounded) is only possible when a galvanically isolated test control device is utilized. Otherwise the plus and minus pole of the isolation test control device will be shorted.

Please note: Because of safety measures during and after the test procedure the heat sink should be grounded: if the DUT fails with an arcing and if the test control device recognizes it and disconnects from the DUT, it is possible the DUT is still electrically charged. In this case it would be dangerous to touch the DUT after the test procedure. In addition to this without grounding the test voltage could drift and the voltage to ground will be even higher than the nominal test voltage.

All isolation voltage tests must be performed at an ambient temperature of 15…35°C, a relative humidity of 45…75% and an atmospheric pressure of 860…1060 hPa. The standards do not define a certain leakage current value and, thus, the isolation test (dielectric test) is considered passed if no electrical breakdown has occurred, i.e. small leakage currents that occur are irrelevant.

There are two forms of an isolation damage:

1. Complete breakdown (according the standards)
2. High leakage current (not according the standards!)

According to the corresponding standards it is required to do an IVT with AC voltage. In contrast the IVT with DC voltage is recommended because in case of an AC IVT high leakage currents lead to an uncertain identification of the isolation problem.
It is recommended to ramp up the isolation voltage with 10kV/s. Faster ramp up leads to capacitive leakage currents and could cause the faulty activation of the isolation test control unit. Slower ramp up leads to a longer testing time. The start of the testing time of 1s as specified in the data sheet begins when the full isolation voltage is reached. The isolation voltage could be switched off without a ramp down. After finishing the test it must be checked that the DUT is not charged anymore.

Please note: The isolation test voltage should not be higher than necessary for the application and stipulated in corresponding standards.

The isolation measurement is performed in two steps:

1. high voltage isolation test
2. repeated isolation test

The high-voltage isolation test and repeated test of an isolation barrier can degrade the isolation capability due to partial discharge. During the IVT since the isolation voltage is applied the partial discharge starts after the voltage goes beyond the partial discharge inception voltage. The higher and the longer the voltage value is applied, the stronger the damage of the isolation through the partial discharge will be. Thus each IVT leads to a weakening of the isolation. Partial discharge in the DCB doesn't lead to a weakening of the isolation, because the ceramic substrate is robust against partial discharge. First of all the organic materials (plastic) e.g. circuit boards and compound of transducers will be damaged.
Since every isolation test may cause a premature damage to the module as a result of partial discharge, the number of tests should be kept low. If they can not be avoided, however, a regeneration time of at least 10 minutes must be kept between 2 subsequent tests and the repeated isolation voltage tests should be performed with reduced voltage. The test voltage must be reduced by 20% for each repeated test.

Please note: The F-option must be removed during the IVT (mounting instruction on request). Then the normal test procedure as above described should be performed.

7.7 Current sharing between paralleled half bridge modules

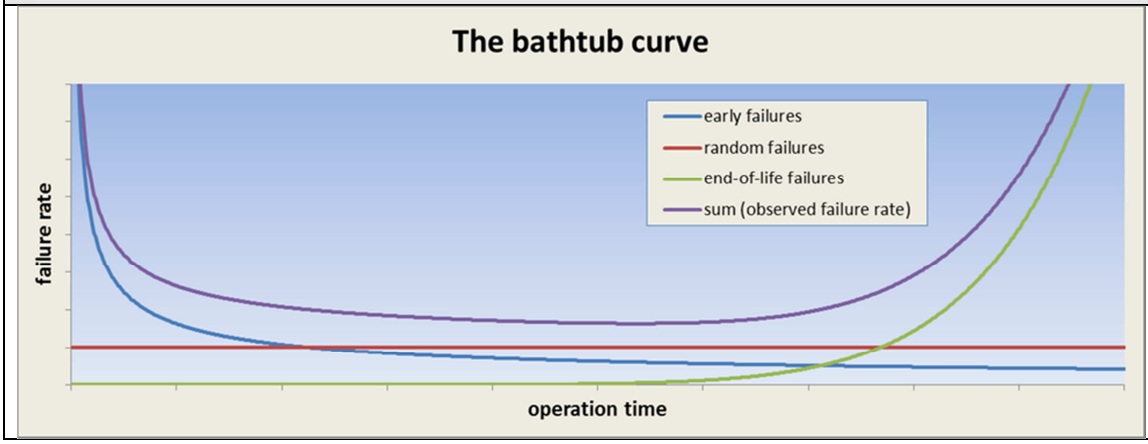
The busbar design has to bedesigned symmetrically to make sure that the current sharing is equal. Unequal current sharing can overload single half bridge modules and leads to imbalance during switching operation as well as in steady state conduction which can finally destroy the power section.
Symmetrical AC and DC-link design leads to equally balanced stray inductances between the half bridge modules which ensures almost equal commutation and current sharing. Each half bridge module has to have the same stray inductance to the DC-link capacitors, too.
The current sharing should be measured in the design phase by "double pulse testing" (see AN-7006) and in the final design under real operation conditions. This can be done e.g. by Rogowski current sensors which are located around the DC+ and DC-terminals.

7.8 Recommended temperature rating

Please note: The compliance of temperature characteristics recommended in this chapter are extremely important for the SKiiP®3 V3 reliability and therefore for the long life time of the product.

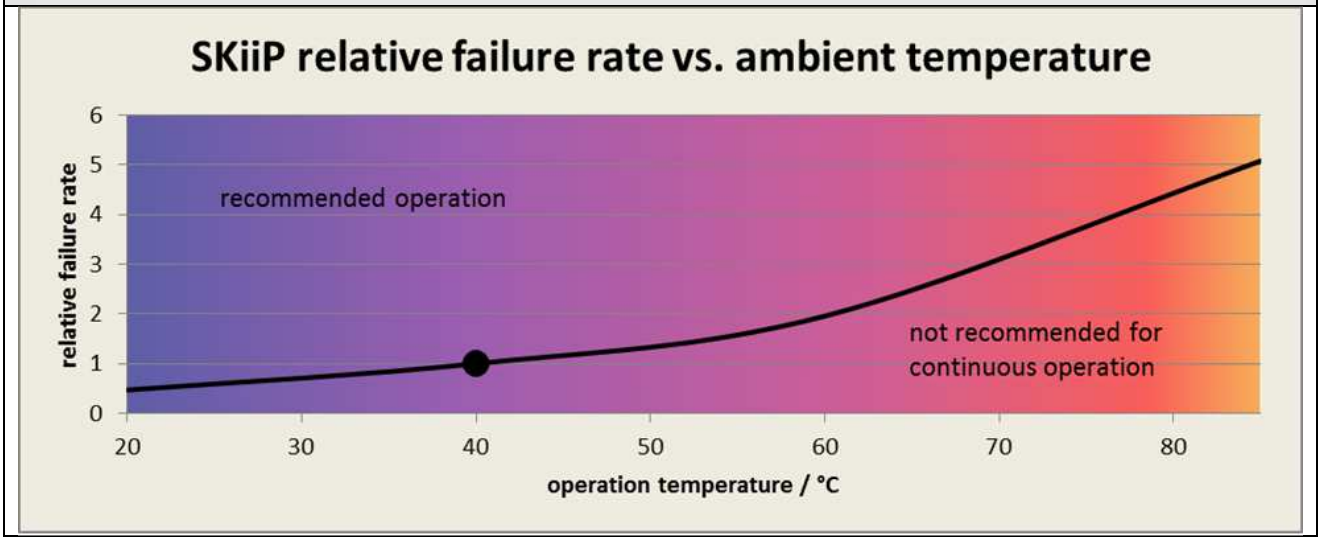
The failure rate describes the probability of a failure within a certain time. Usually, the failure rate follows the so-called bathtub curve, shown in Figure 7.7: high in the beginning (failures known as early failures), then dropping to a low and more or less constant value (the random failures) before it rises again as wear-out begins to set in and end-of-life failures set a limit to the useful life of a component.

Figure 7.7: Probability of a failure during operation time.



The evaluation of the failure rate for different temperatures shows that its expected failure rate roughly doubles for a 20 C increase in operating temperature (see Figure 7.8).

Figure 7.8: SKiiP driver failure rate temperature dependence calculated according to SN29500



The less stress a device is subjected to, the less likely it is to fail. Low operation time, low current, low temperature and low DC-link voltage prolong its life and reduce the failure rate. Therefore, the design has to find a working compromise between exhausting a device to maximum capacity and obtaining an acceptable failure rate and life time.
The following temperature rating is recommended for the SKiiP®3 V3 systems:

1. Power section: It is necessary to make sure by calculations and measurements that the recommended IGBT and diode junction temperatures are not exceeded also considering overload conditions. The recommended maximum junction temperatures are 125°C which is 25°C lower than the maximum temperature of 150°C. That is to ensure the reliable operation. Calculations can be carried out by the SEMIKRON simulation tool SEMISEL which is available on the SEMIKRON homepage www.semikron.com. Load cycles and cooling conditions can be adapted to meet the application conditions. Measurement of the DCB-sensor temperature (available on the driver connector as analogue voltage signal) has to be carried out to check that the system works as calculated: if the DCB-temperature value coming from SKiiP®3 V3 during the real operation is close to the heat sink temperature given in the results of SEMISEL calculation, then the calculated chip temperature is also very close to the real chip temperature.
2. Gate driver: Although it is possible for an operation at 85 C, it is recommended that the average ambient temperature of the driver board does not exceed 40 C for extended periods of time. For achieving a lower driver temperature an additional air forced cooling for the driver might be necessary.

7.9 Paralleling of SKiiP®3 V3

For a parallel operation the following should be implemented:

- common error management for all paralleled SKiiP®3 V3
- monitoring of analog signals, e.g. temperature or current
- one power supply should be used for all subsystems
- decoupling reactors

The easiest way to make the paralleling of SKiiP®3 V3 is to use the Parallel Board SKiiP®3 V3, where all these points, except the decoupling reactors, are already implemented and tested. For further information about the Parallel Board SKiiP®3 V3 please refer to the Technical Explanation SKiiP®3 Parallel Board.

By using paralleled SKiiPs it has to be made sure that each paralleled SKiiP will not be overloaded. To ensure this a potentially occurring imbalanced current sharing between the paralleled SKiiP's has to be limited. This inhomogeneous current is caused by different output voltages of the paralleled inverters which could be a consequence of:

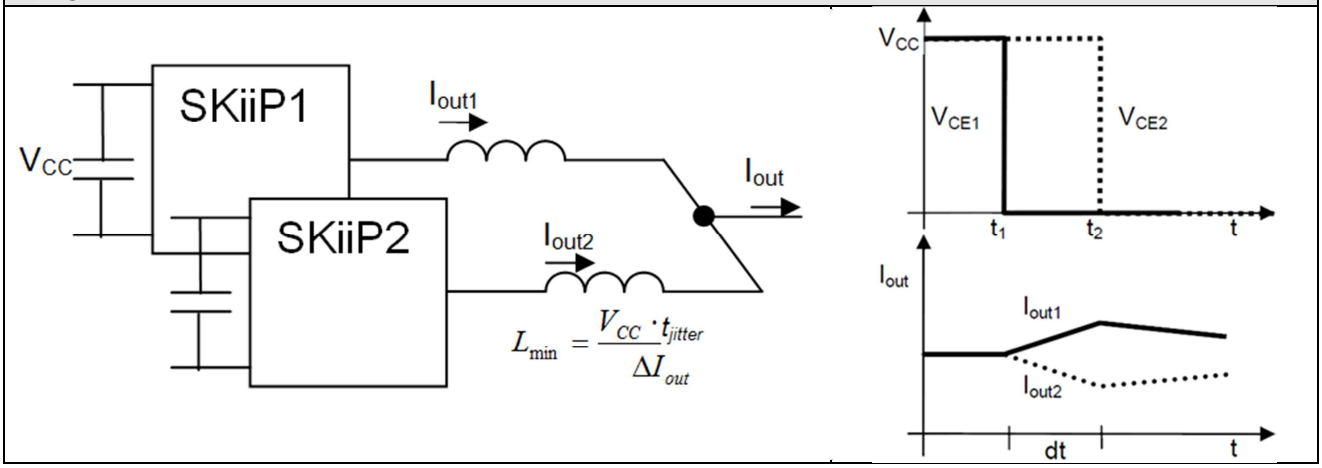
- different propagation time delay of driver boards

- different switching times of power semiconductors
- tolerance of forward voltage drop of IGBT and diodes
- different DC link voltage levels
- different cooling conditions of paralleled half bridges (e.g. in air cooled applications with thermal stacking)
- different external impedance

To minimize these effects the system designer has to ensure, that there is sufficient inductance between the AC output terminals of the paralleled SKiiP subsystems. The impedance has two tasks:

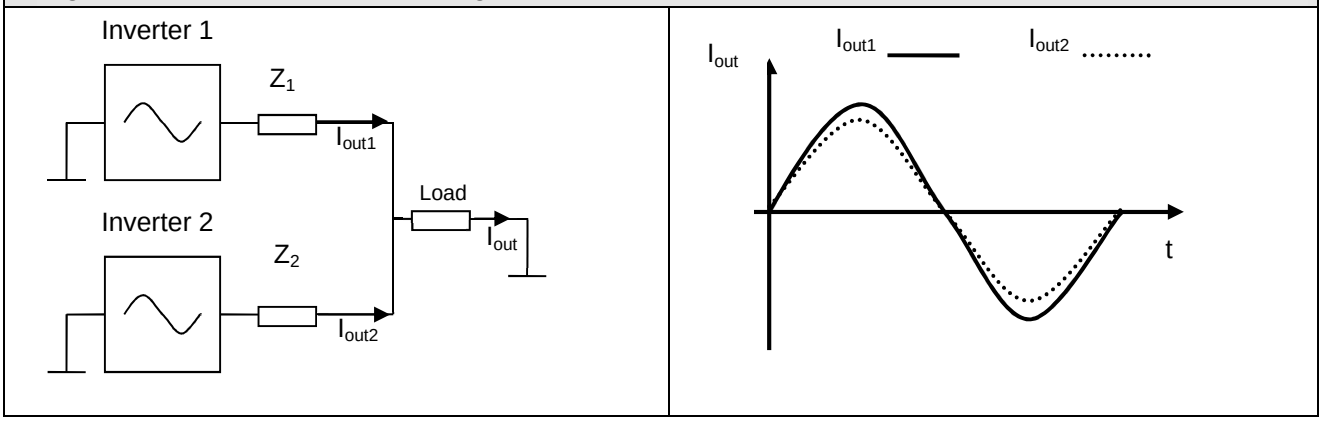
- On the one hand it should prevent the divergence of the current during the switching moment. That could lead to dynamic overload, respectively to oscillations. This is shown in Figure 7.9. The value t_{jitter} is given in the SKiiP®3 V3 data sheet, page 2.

Figure 7.9: Effects of paralleling SKiiP®3 V3



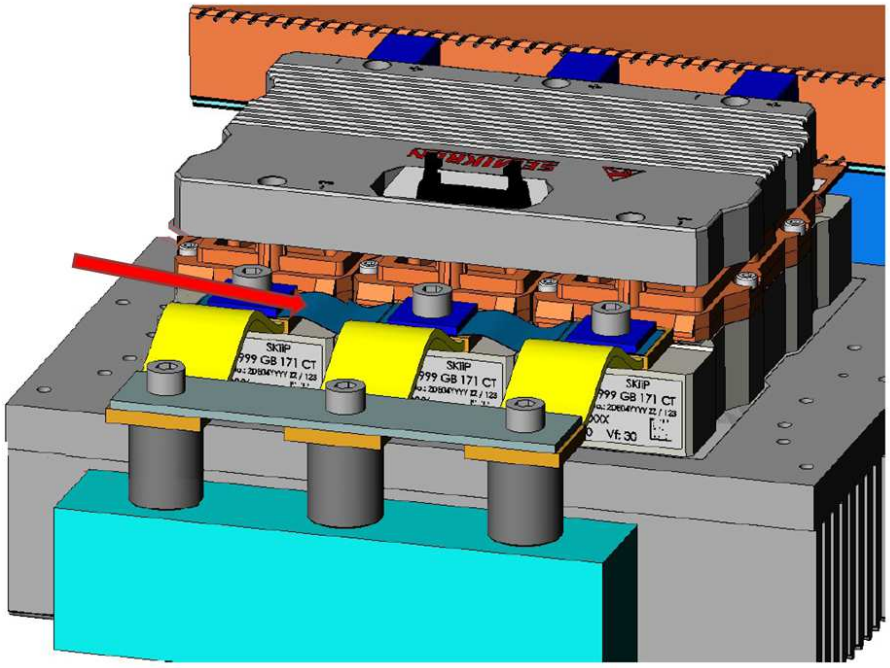
- On the other hand a different root mean square value of the output current should be avoided. Symmetric effects come from the inductivities (AC choke) and the ohmic resistors (choke resistor, wiring resistor and path resistance) as shown in Figure 7.10.

Figure 7.10: Schematic Circuit Diagram



A low inductive parallel connection of the AC-terminals can be achieved by an additional flexible cross connector directly mounted on the SKiiP AC terminals (see Figure 7.11). Please note that the current rating of this bar must not be very high, because there is no static load current flowing in this bar. Hence, there are only high frequency currents flowing. Thus the flexibility can be achieved by using a comparatively thin material.

Figure 7.11: Example of AC cross connector



Tolerance of forward voltage drop of IGBT or diodes
The IGBTs used in the SKiiPs have a positive temperature coefficient. The free wheeling diodes are produced with a small forward voltage range. Both limit the inhomogeneous current distribution. No further selection of forward voltage groups is necessary.
Different DC link voltage levels
To avoid different output voltages caused by different DC link voltages levels, the DC link should be connected in parallel. It has to be avoided that oscillations between the capacitor banks occur. For large systems fuses between the capacitor banks are recommended. The paralleled systems should have the same DC link with the same capacitor type and capacitor values.
Different cooling conditions of paralleled half bridges
The cooling system of the paralleled SKiiP units should be designed in a way to avoid thermal stacking.
In spite of all the mentioned actions it has to be taken into account that for inhomogenous current sharing a derating of the nominal current of the power section has to be considered.

7.10 Prevention of condensation

Condensation during operation must be prevented. This can be ensured by a suitable regulation of the air or water flow so that the heat sink temperature is always above the ambient temperature. The use of chilled coolant is therefore not recommended. Condensation may occur because of night/day temperature change as well.
If the power electronic equipment was exposed to humidity or moisture during transport and storage, it should be dried before commissioning. This can be done by air heater in air cooled systems or by pre-heated water in water cooled systems.

8. Logistics

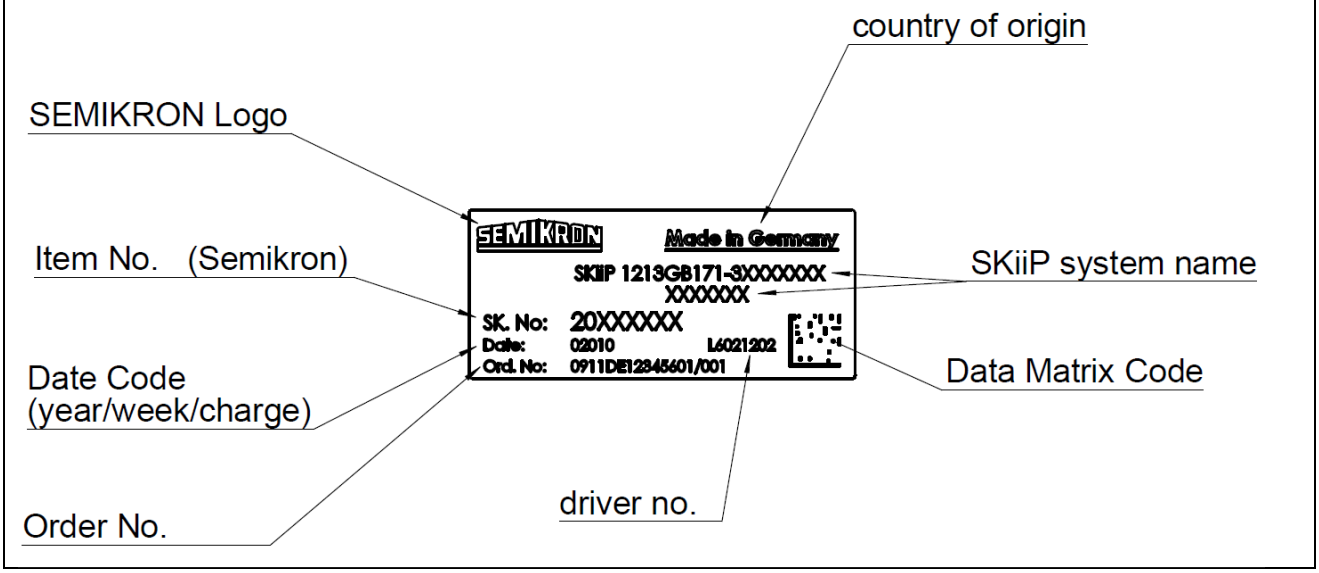
8.1 Label

For reasons of traceability all SKiiP®3 V3 modules are marked with a system, halfbridge, driver shuttle and a warranty label.

8.1.1 System Label

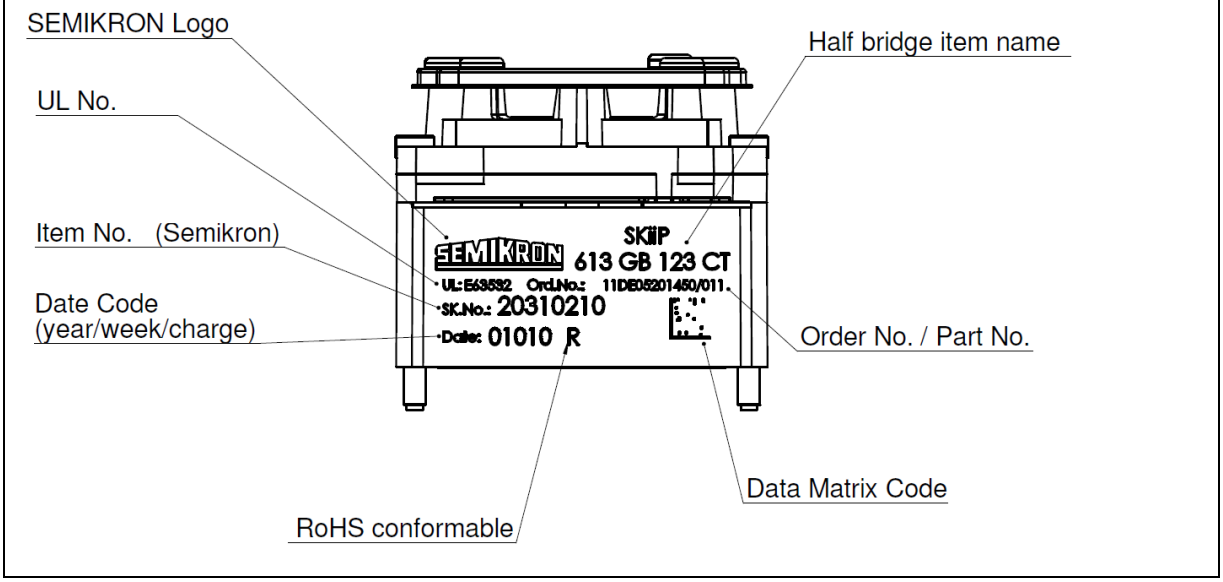
The system label of SKiiP (Figure 8.1) is the label which contains all information necessary for customers. In case of technical inquiries please always name the SKiiP Item number written on this label.

Figure 8.1: System Label of SKiiP®3 V3



8.1.2 Half bridge Laser Label

Figure 8.2: Half bridge label of SKiiP®3 V3



8.1.3 Warranty Label

The warranty label is shown in Figure 8.3. The position of the warranty label can be found in the corresponding data sheet.

Figure 8.3: **Warranty Label of SKiiP®3 V3**

Please note: Removing the warranty label will result in loss of warranty in case of product claim.

8.1.4 Data Matrix Code

The Data Matrix Code is described as follows

⇒ Cell size: 0,3mm

⇒ Read distance: 60 – 100mm

⇒ Max. angle of 30° (vertical reference line) for reading

Figure 8.4: Data Matrix Code of SKiiP®3 V3

8.1.5 Provisions and handling after use

Components which are obsolete or defective must be disposed according to local regulations

List of figures:

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Abbreviations

Abbreviation	Meaning
CTE	Coefficient of Thermal Expansion
DBC	Direct bonded copper
D-Sub	D-Subminiature
EMC	Electromagnetic compatibility
GB	halfbridge configuration
GND	Ground
IGBT	Insulated Gate Bipolar Transistor
IPM	Intelligent Power Module
PCB	Printed Circuit Board
PTC	Positive Temperature Coefficent
RH	Relative Humidity
RoHS	Restriction of Hazardous Substances
SCP	Short Circuit Protection
SKiiP	Semikron intelligent integrated Power
SPS	Short Pulse Suppression
UVP	Under Voltage Protection

Symbols and Terms

Letter Symbol	Term
I_{Cnom}	Nominal collector current of IGBT
I_{Fnom}	Nominal forward current of diode
$I_{digiout}$	Digital output sink current (HALT-signal)
Q_{PD}	Charge of the Partial Discharge event
$R_{CC´+EE´}$	Resistance of the interconnections between terminals and die
R_{th}	Thermal resistance
$t_{pReset(OCP)}$	Overcurrent reset time
t_{jitter}	Jitter clock time
t_{SIS}	Short pulse suppression time
t_{bl}	Blanking time
t_{POR}	Power-On Reset time
T_a	Ambient temperature
T_j	Junction temperature
T_r	Temperature at reference position
U_{LE}	Line to earth voltage
U_{LL}	Line to line voltage
V_{CEstat}	Collector-Emitter Threshold Static Monitoring Voltage
$V_{it+\ HALT}$	Input threshold voltage HALT-signal (HIGH)
$V_{it-\ HALT}$	Input threshold voltage HALT-signal (LOW)
$T_{DriverTrip}$	Over temperature trip level
$f0_{Uana}$	Bandwidth of DC-voltage measurement @ V_{DCtrip}
$f0_{Iana}$	Bandwidth of current measurement @ I_{TRIPSC}
$f0_{Tana}$	Bandwidth of temperature measurement @ T_{trip}

A detailled explanation of the terms and symbols can be found in the "Application Manual Power Semiconductors" [2]

References

[1] www.SEMIKRON.com
[2] A. Wintrich, U. Nicolai, W. Tursky, T. Reimann, “Application Manual Power Semiconductors”, ISLE Verlag 2011, ISBN 978-3-938843-666

HISTORY

SEMIKRON reserves the right to make changes without further notice herein

2.0	Technical documentation revised
3.0	Update Table 4.4 and Chapter 6
4.0	Chapters 7.3 and 7.4 added, Chapter 5.3.7.2 updated

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