SIEMENS

SIMATIC NET

PROFIBUS Controller SPC 4®-2 LF

Manual

C79000-G8976-C157-3

Release 12/2006

Contents

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Contents

Introduction 1

ASICs

For simple and fast digital exchange between programmable logic controllers, Siemens offers users various ASICs. These ASICs either support or handle the entire data exchange between the automation stations according to the PROFIBUS standards and guidelines DIN 19245 Part 1, Part 2, Part 3 and PROFIBUS PA (Part 4), EN 50170 Volume 2, IEC 61158 Ed.3, and IEC 61784-1. The SPC 4®-2 also supports the Foundation Fieldbus as described in IEC 61158. Ed3.

Functionality

The **SPC 4®-2** (**S**iemens **P**ROFIBUS **C**ontroller) operates at layer 1 of the OSI model and requires an additional microprocessor to implement layers 2 and 7.

With the **SPC 4®-2** , parts of layer 2 that handle the bus protocol are integrated. For the other functions of layer 2 (interfacing, management) an additional microprocessor is required.

In addition to the layer 2 functionality, the following productive services are also integrated on the ASIC: Data_Exchange, Read_Input, Read_Output and the Global_Control command of DIN E 19245 Part 3/EN50170/IEC61158 as well as the PROFIBUS-PA functionality (DIN E 19245 Part 4/EN 50170/IEC 61158, IEC 61784-1).

SPC 4-2 supports the following communication profiles:

- PROFIBUS FMS
- PROFIBUS PA
- PROFIBUS DP
- Foundation Fieldbus®[1] (FF).

The communication profiles and the possible combinations with the physical media (copper, glass-fiber) are described in the IEC 61784-1 standard (apart from PROFIBUS-FMS, see EN 50170 Vol. 2).

The SPC 4-2 supports passive nodes on the bus system (slaves) and filters out all external frames and bad data frames.

To extend the SPC 4-2 for PROFIBUS PA and FF, the SIM 1 communication interface chip is available. The SIM 1 ASIC implements the function of a Medium Attachment Unit (MAU).

[1] Foundation Fieldbus is a registered trademark of Fieldbus Foundation.

Functional Overview 2

Apart from the bus drivers, the SPC 4-2 contains the entire PROFIBUS peripherals. The additional processor does not need to provide a hardware timer to process the bus protocol.

Baud rates from 9.6 kbit/s to 12 Mbit/s are supported. The SIM 1 ASIC is an ideal extension for PROFIBUS PA.

The SPC 4-2 has a universal microcontroller interface with an 8-bit data bus interface and a 10-bit address bus. Depending on the configuration, the data/address but can be operated separately or multiplexed so that processors with the standard x86 timing, the Motorola timing, the SAB C165 timing, or an 80C32 timing can be connected.

Since the interface supports both INTEL and MOTOROLA architectures, the Intel or Motorola data format is selected with two configuration pins along with the synchronous (rigid timing) or asynchronous (with Ready support) processor bus timing.

The handshake between the processor and the SPC 4-2 is executed by the FLC firmware (Field Bus Link Control; synonym for all communication stacks) via the dual-port RAM (extended to 3 Kbytes) integrated on the SPC 4-2.

From the point of view of the user, the SPC 4-2 occupies an address space of 1 Kbyte.

The plausibility check when request frames are received is handled by the SPC 4-2.

Pulse Modulation

The SPC 4-2 has circuits for a direct connection SIM 1-optocoupler-SPC 4-2 (PROFIBUS PA attachment) using the current-saving interface of the SIM. A separate adapter circuit is no longer necessary.

The frames received from the SIM 1 are converted to a series of short pulses and then passed on to the SPC 4-2.

Fast Synchronizer in the Manchester Receiver

Fast synchronization means finding the bit mid point in the preamble of a Manchester frame (PROFIBUS PA). This allows the SPC 4-2 to tolerate larger systematic distortion (all rising or falling edges are delayed by the same amount).

Compatibility with SPC 4/4-1

The SPC 4®-2 is compatible with the ASIC SPC 4® and SPC 4®1. This compatibility includes the mechanical and electrical properties as well as the functions used via a software interface.

Additional properties of the SPC 4-2

- Optional use of PROFIBUS and Foundation Fieldbus by changing the firmware
- *PROFI*Safe prepared (slave-slave communication)
- *PROFI*Drive support (clock pulse output)
- Time-of-day synchronization for time stamping alarms and events
- Memory expanded from 2K to 3K
- Diagnostic output
- Selectable unsharpness window of the pulse modulation

The expansions of the SPC 4-2 are activated using previously unused parameter registers. The SPC 4/SPC 4-1 does not evaluate address bits 7 to 5 when the parameter registers are accessed so that all registers can be accessed under several addresses (write and read). All the SPC 4/SPC 4-1 and 4 new SPC 4-2 registers are within this accessible address space. By activating the "Enable SPC 4-2" bit, the SPC 4-2 evaluates all address bits.

The SPC 4-2 contains 4 new 16-bit timers. These can be used in the FF mode since they use interrupt bits that are only free in the FF mode. All the timers are clocked at the baud rate and can be operated as "One-Shot" or as "Cyclic" timers.

Additional properties of the SPC 4-2 LF

- Meets the requirements of the EU directive:
  2002L0095 — EN — 01.07.2006 — 002.001 — 1
- Can be used with lead-free and lead solder techniques
- New package type 44-pin LQFP
- New delivery packaging

Pin Assignment

3

The SPC 4-2 has a 44-pin *plastic quad flat package* housing (see Chapter 11). The pin assignment is described in Table 3-1 Pin Assignment

Note:
All signals that start with X.. are LOW-active

Pin	Signal name	In/ Out	Description	Source / Dest	Processor Variant
1	XCS	I	Chip select	CPU	C32 mode: connect to VDD otherwise: CS signal
2	XWR / E	I	Write signal E-clock with Motorola 1 clock pulse=1 memory cycle (in asynchronous mode, connect to VDD)	CPU	
3	DIVIDER	I	Divider for ISCLK-OUT (pin 7) 0=:4, 1=:2	System	
4	XRD R/W	I	Read signal Read/Write with Motorola (low=write)	CPU	
5	CLK	I	Clock input	System	
6	**VSS**				
7	ISCLK-Out	L	Input clock, divided by 2 or 4	System, CPU	
8	Type	I	Data format of processor interface (see Mode Table)		
9	XINT	L	Interrupt output	CPU, Interrupt-Contr.	
10	XINTCI	L	Port pin in the compatibility mode, in the extended mode interrupt output clock synchronization	CPU, Interrupt-Contr.	Port pin bit 1 of mode register 2
11	DB0	I/O	Data bus	CPU, memory	C32 mode: data/address bus multiplexed Otherwise: data/address bus separate
12	DB1	I/O	Data bus	CPU, memory	
13	XHOLDTOKEN	L	Port pin in compatibility mode, in extended mode trigger output for measurements		Port pin bit 0 of mode register 2
14	XREADY XDTACK	L	Ready for external CPU Data transfer acknowledge with Motorola	System, CPU	
15	DB2	I/O	Data bus	CPU, memory	C32 mode: data/address bus multiplexed Otherwise: data/address bus separate
16	DB3	I/O	Data bus	CPU, memory	
17	**VSS**				
18	**VDD**				
19	DB4	I/O	Data bus	CPU, memory	C32 mode: data

Pin	Signal name	In/ Out	Description	Source / Dest	Processor Variant
20	DB5	I/O	Data bus	CPU, memory	/address bus multiplexed
21	DB6	I/O	Data bus	CPU, memory	Otherwise: data/address bus
22	DB7	I/O	Data bus	CPU, memory	separate
23	MODE	I	Timing format of the processor interface (see Mode Table)	System	
24	ALE AS	I	Address latch enable Address strobe with Motorola (in synchronous operation connect to VDD)	CPU	C32 mode: ALE Motorola mode AS
25	AB9	I	Address bus	CPU	C32 mode: : <log> 0
26	TXD-TXS	L	Serial transmit channel	RS-485 transmitter	
27	RTS-ADD	L	Request To Send	RS-485 transmitter	
28	**VSS**				
29	AB8	I	Address bus	System, CPU	C32 mode: <log> 0
30	RXD-RXS	I	Serial receive channel	RS-485 receiver	
31	AB7	I	Address bus	System, CPU	C32 mode: <log> 0
32	AB6	I	Address bus	System, CPU	C32 mode: <log> 0 for CS
33	XCTS	I	Clear to Send <log> 0 = clear to send	MODEM/FSK	
34	XTEST0	I	Pin must be connected to VDD.		
35	XTEST1	I	Pin must be connected to VDD.		
36	RESET	I	Reset input: connect to port pin of CPU		
37	AB4	I	Address bus	System, CPU	C32 mode: <log> 0 for CS
38	**VSS**				
39	**VDD**				
40	AB3	I	Address bus	System, CPU	C32 mode: <log> 0 for CS
41	AB2	I	Address bus	System, CPU	C32 mode: <log> 0 for CS
42	AB5	I	Address bus	System, CPU	C32 mode: <log> 0 for CS
43	AB1	I	Address bus	System, CPU	C32 mode: address window
44	AB0	I	Address bus	System, CPU	C32 mode: address window

Table 3-1 Pin Assignment

Memory Assignment

4

4.1 Addressing the SPC 4-2

From the user perspective, the 3-Kbyte internal dual-port RAM and the internal latches occupy a 1-Kbyte address space. Parts of the internal RAM are located directly in the address range of the microprocessor, the other parts can be addressed using a window mechanism, see Figure 4-1

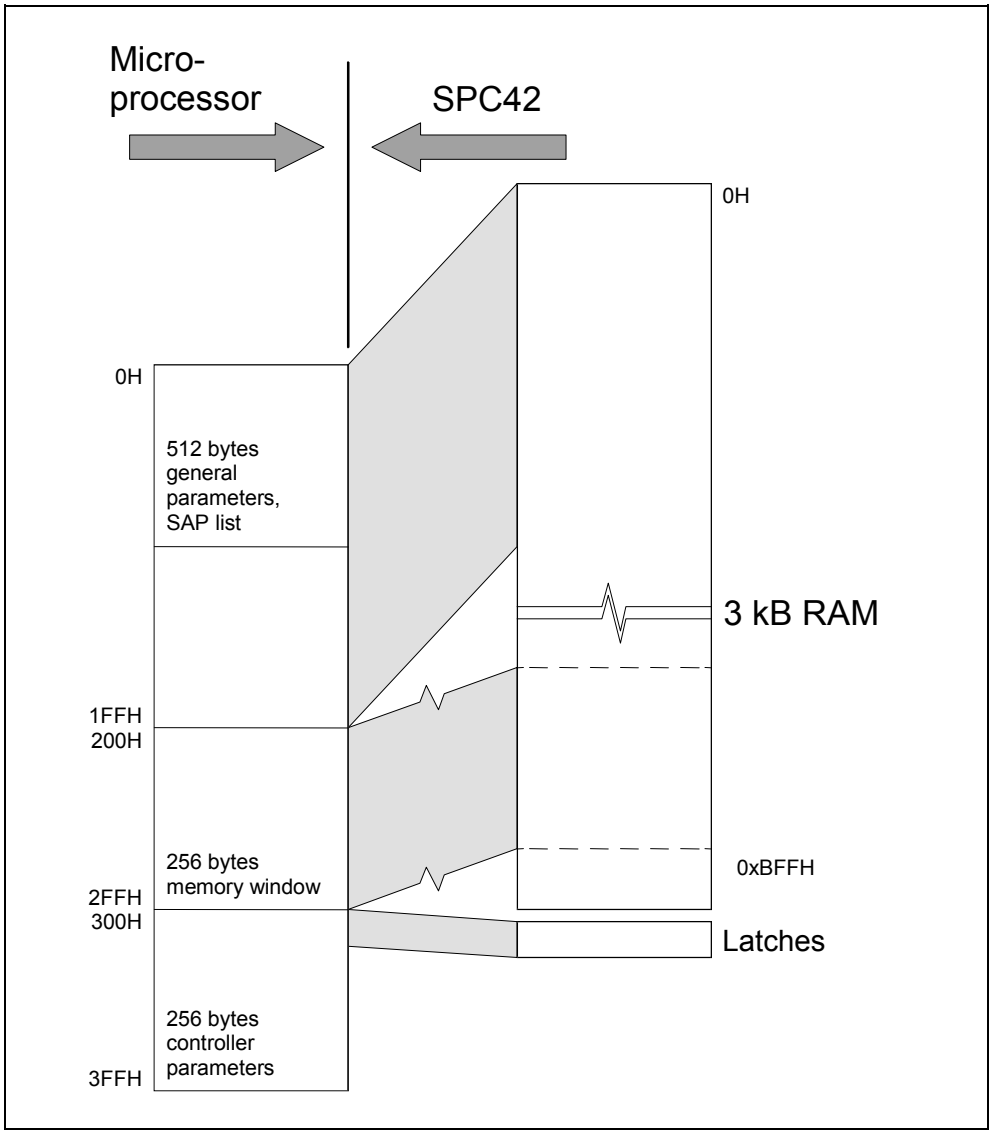

Figure 4-1 Addressing the Internal 3-Kbyte RAM

Address Window

With the lower address window, the FLC can access the first 512 (2 x 256) bytes of the RAM physically without needing to load the base pointer. The advantage of this is that the FLC can access the general parameters or the SAP list directly without first needing to load the base pointer.

The entire internal memory can be addressed via the second address window of 256 bytes (200h to 2FFh) with the aid of an 8-bit base pointer. This pointer must be loaded by the FLC and always addresses the beginning of an 8 byte segment (in the extended SPC 4-2 mode, 16 bytes). This means that the FLC can address up to 256 bytes using the offset address applied to the address pins of the SPC 4-2.

The third address window which is also 256 bytes long (300h to 3FFh) is used to address the internal latches required for direct control of the hardware. These latches are not integrated in the internal RAM area!

Address bit A9	Address bit A8	Window Select
0	0	Parameter area (physically 00h-FFh)
0	1	Parameter area (physically 100h-1FFh)
1	0	Entire RAM using base pointer
1	1	Parameter register

Table 4-2 Window Select

Notice:

Overwriting the address area is not prevented by the hardware; in other words, if the user writes beyond the node table, the parameters are overwritten in the lower memory area due to the "wraparound" function. In this case, the SPC 4-2 generates the Mem-Overflow interrupt.
If read-only parameters are written to, an access violation interrupt is generated.

4.2 Structure of the Internal RAM

4.2.1 Overview

Figure Figure 4-3 shows the structure of the internal 3 Kbyte RAM of the SPC 4-2. The entire memory area made up of segments of 8 bytes (or 16 bytes in the extended SPC 4-2 mode) is divided into different areas.

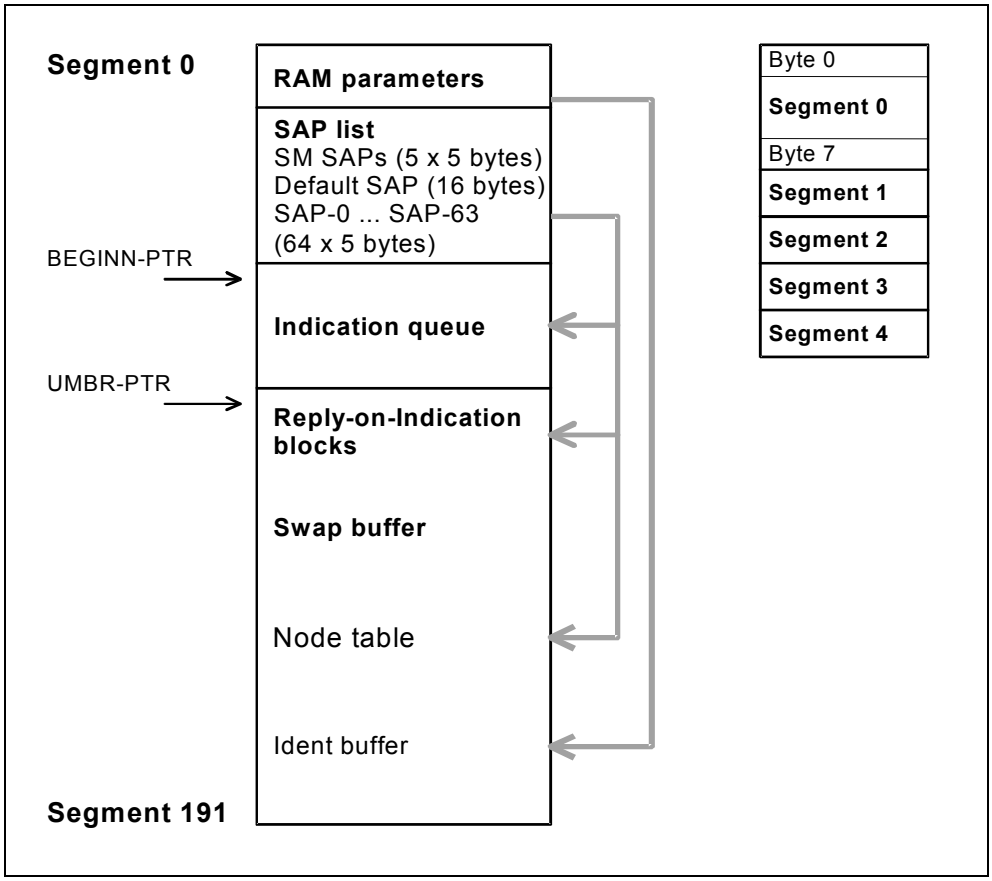

Figure 4-3 Memory Structure

4.2.2 RAM Parameter Block

The first 6 or 8 bytes of the integrated RAM contain the general parameters such as the read and write pointers of the indication queue that do not intervene directly in the controller, see Table 4-4. The FLC is permitted to write only the parameters with addresses 00H to 5H or 7H. The internal working cells must not be overwritten (the hardware generates a write-violation interrupt and goes offline).

Address	Name	Access	Meaning	
00H	IND-WP-PRE	RD/WR	The write pointer for indication preprocessing points to the next free segment that follows the last request frame received even when no indication "IND" has been received. The IND-WP-PRE pointer allows a fast slave reaction (for example for PROFIBUS DP). The IND-WP-PRE pointer is set to the next free segment boundary immediately after receiving a request frame correctly (even before a response frame is sent). At the same time, the "IND-PRE" interrupt is generated. This pointer must not be changed by the FLC.	
01H	IND-WP	RD/WR	Write pointer of the indication queue pointing to the next free segment following the last indicated request frame. With each "IND" indication interrupt, IND-WP is set to a new segment boundary by the SPC 4-2. This pointer must not be changed by the FLC.	
02H	IND-RD	RD/WR	The read pointer of the indication queue is also a segment address and is managed by the FLC.	
03H	FDL-Ident-Ptr	RD/WR	Pointer to the Ident buffer	
04H	TS-ADR-REG	RD/WR	Contains the node address	
			PROFIBUS PA	
			0 … 119	Normal node
			120..124	Temporary node (for example handheld)
			125	Default address for temporary nodes
			126	Default address for permanent nodes
			127	Broadcast/multicast
			PROFIBUS DP	
			0 … 125	Normal node (recommended for slave: 3..125)
			126	Default address for address assignment
			127	Broadcast/multicast
05H	SAP-MAX	RD/WR	The highest SAP list number is set	
06H	AQUI-ADR	RD/WR	Station address of the valid constant bus cycle time master (exists only in SPC 4-2 mode, otherwise a write violation interrupt is generated in response to write access)	
07H	GRP-BYTE	RD/WR	Group selection byte for clock synchronization (exists only in SPC 4-2 mode, otherwise a write violation interrupt is generated in response to write access)	
08H..17H	Internal work cells		The following cells must not be overwritten (write-violation interrupt)	

Table 4-4 Assignment of the RAM Parameter Block

Access to the parameter registers or the internal RAM require not only the correct connection of the relevant address bits but also the connection of an XCS signal to the SPC 4-2. In addition to this, the XREADY signal of the SPC 4-2 must be taken into account or suitable wait states must be created.

Note

When writing the RAM parameters, the upper unused bits must be set to '0' while the unused bit positions in the parameter registers are 'don't care'.

4.2.3 SAP List

The SAP list can be addressed directly and no segmentation or use of the base pointer is required although it is also possible to use the base pointer for addressing. To access the data to which a SAP points, the base pointer must be used.

The area of the service access points (SAPs) occupies 361 bytes (address 18H .. 180H). The SAP list is made up of the following:

- 5 SM-SAPs (System Management Service Access Point) each 5 bytes long
- DEFAULT-SAP (Service Access Point) with 16 bytes
- 64 SAPs each 5 bytes long

Table 5-1 shows the SAP list, the functions of the individual registers and bits are explained in the following sections.

4.2.4 Data Areas in the Internal RAM

Indication Queue

Following the SAP list, there is a memory area for the indication queue. The address area can be set at segment boundaries by the FLC. The first possible address in the compatibility mode (8 byte segment size) is 188H, in the extended SPC 4-2 mode it is 190H.

The BEGIN-PTR is the address of the first segment of the indication queue. The end of the queue is indicated by UMBR-PTR. The UMBR-PTR points to the address of the first segment that **no longer** belongs to the indication queue.

Caution

After initialization in the offline mode, both pointers must be set to the required start of the range. THEY CANNOT BE MODIFIED DYNAMICALLY; in other words, to modify the memory assignment, the SPC 4-2 must be changed to offline. A change in the order of the pointers leads to an incorrect response of the SPC 4-2 related to the individual memory areas.

If the SPC 4-2 receives request frames, it enters them in the indication queue. The indication queue is organized as a ring buffer; in other words the data to be processed is entered one after the other in the queue as long as there is still space in the queue and blocks that have been processed are taken out of the queue. The indication queue is organized using write and read pointers. The indication read pointer (IND-RP) must be set by the FLC while the hardware of the SPC 4-2 is responsible for updating the indication write pointer (IND-WP).

Since this is a ring buffer, the end of the queue must be monitored when data are entered. If this is exceeded, the address must be wrapped. The SPC 4-2 provides hardware support that automatically wraps the address.

Reply-on-Indication Blocks

The FLC must provide reply data in these buffers. The reply data are assigned to the calls using pointers in the SAP lists.

Swap Buffers

To support PROFIBUS DP services (DP mode = 1 in the mode register 0), 6 swap buffers must be provided.

Ident Buffer

The Ident buffer contains the reply data for Ident frames.

Node Table

The node table is required to filter SDN or DDB response frames.

4.2.5 Addressing Using the Memory Window

When addressing the SPC 4-2, the physical address of the integrated RAM is formed via the second address window (200h to 2FFh) from the base pointer, the segment address for the indication queue and the lower 8 bits of the address bus. The base pointer is added to the address of the address that is shifted by three or four bit positions, see Figure 4-5.

In the extended SPC 4-2 mode, the base pointer is shifted by 4 bits instead of by 3 bits to the left so that the segment size is then 16 bytes instead of 8 bytes.

New segment address = base pointer + AB7..3 - end pointer + begin pointer

8-byte segment in the compatibility mode

New segment address = base pointer + AB7..4 - end pointer + begin pointer

16-byte segment in the SPC 4-2 mode

Along with the 3 or 4 least significant address bits, the result forms the physical 11-bit or 12-bit address for the internal RAM. With the calculator, the FLC can address up to 256 data bytes once the base pointer is loaded without having to reload the base pointer or worry about the wrapping at the queue limit.

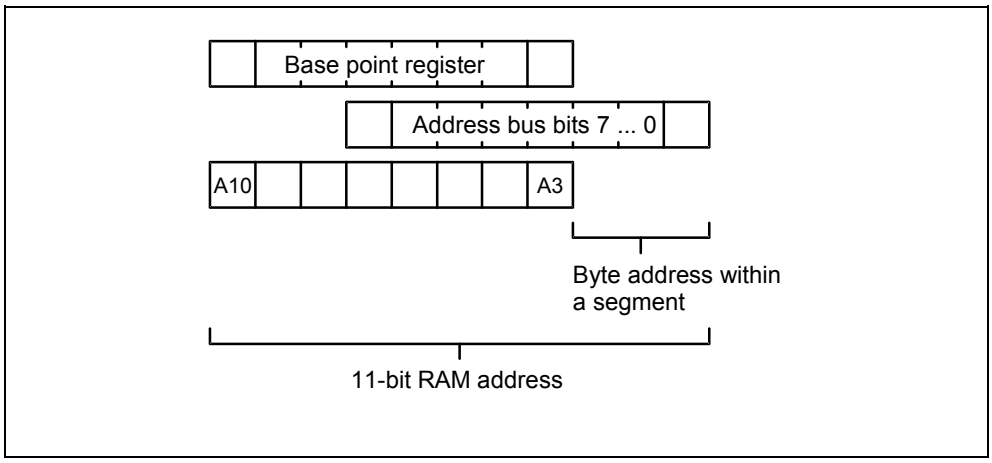

Figure 4-5 Calculating the Physical RAM Address in the Compatibility Mode

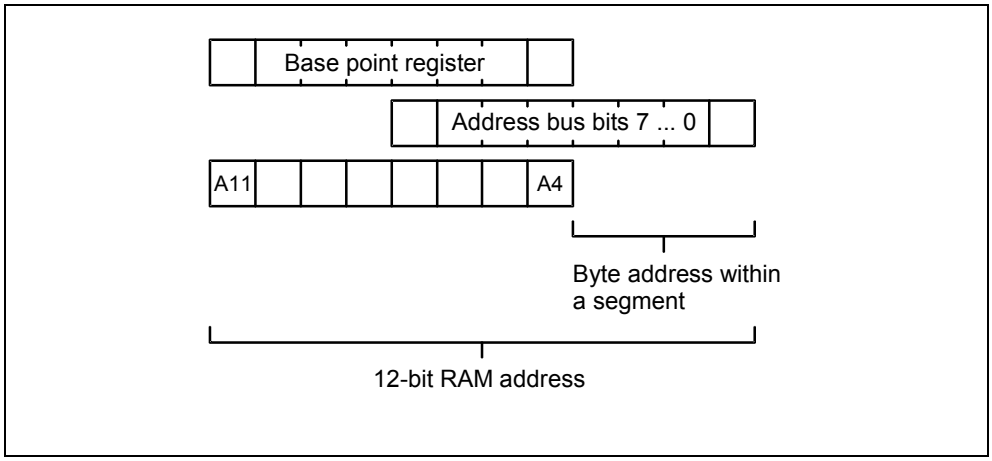

Figure 4-6 Calculating Physical RAM Address in the Extended SPC 4-2 Mode

4.3 Assignment of the Parameter Registers

It is only possible to access the internal parameter registers (in other words, the memory cells that intervene directly in the controller) using the address window 300h to 3FFh on the SPC 4-2.

These cells can either only be read or only be written and have different functions. In the Motorola mode, the SPC 4-2 swaps addresses for access to the address range starting at 300H (word register); in other words, it swaps the address bit 0 (generates an odd address from an even address and vice versa).

The SPC 4-2 has an 8-bit data interface. When the byte registers are accessed via this interface, it does not matter whether the SPC 4-2 is in the Intel or in the Motorola mode.

When the word registers are accessed (two-byte registers), the SPC 4-2 distinguishes between the Intel and Motorola mode.

Example: INT-MASK-REG

Intel mode: Write access with address 300
⇒ INT-MASK-REG (7..0) is written (little endian)
Motorola mode: Write access with address 300
⇒ INT-MASK-REG (15..8) is written (big endian)

This means that the high byte and low byte are addressed with different addresses.

The meaning of the individual bits in the registers is explained in greater detail in the following sections.

Since the addresses of the parameter registers are not fully coded, the registers appear again every 64 bytes. This simplifies the implementation since different addresses (names) can be assigned for read and write access.

Address Intel	**/Motorola**	**Name**	**Meaning (**READ access !**)**
300_H	301_H	Int-Req-Reg 7..0	Interrupt controller register
301_H	300_H	Int-Req-Reg 15..8	
302_H	303_H	Int-Reg 7..0	
303_H	302_H	Int-Reg 15..8	
304_H	305_H	Status-Reg 7..0	Status Register
305_H	304_H	Status-Reg 15..8	
306_H	307_H	Delay 7..0	Delay timer register, current counter reading
307_H	306_H	Delay 15..8	
308_H	309_H	reserved	
309_H	308_H	reserved	
$30A_H$	$30B_H$	reserved	
$30B_H$	$30A_H$	reserved	
$30C_H$- $30F_H$		reserved	
310_H		Delay 23..16	Extension of the delay timer register
311_H		reserved	
312_H		reserved	
313_H		reserved	
314_H		reserved	
315_H		reserved	
316_H		reserved	
317_H		reserved	
318_H		Mem-Lock 0	Memory lock cell
319_H		reserved	
$31A_H$		reserved	
$31B_H$		reserved	
$31C_H$		reserved	
$31D_H$		reserved	
$31E_H$		reserved	
$31F_H$		reserved	
320_H		Timer0-Reg 15..8	Timer 0 high byte 15...8 (only SPC 4-2 mode)
321_H		Timer0-Reg 7..0	Timer 0 low byte 7...0 (only SPC 4-2 mode)
322_H		Timer1-Reg 15..8	Timer 1 high byte 15...8 (only SPC 4-2 mode)
323_H		Timer1-Reg 7..0	Timer 1 low byte 7...0 (only SPC 4-2 mode)
324_H		Timer2-Reg 15..8	Timer 2 high byte 15...8 (only SPC 4-2 mode)
325_H		Timer2-Reg 7..0	Timer 2 low byte 7...0 (only SPC 4-2 mode)
326_H		Timer3-Reg 15..8	Timer 3 high byte 15...8 (only SPC 4-2 mode)
327_H		Timer3-Reg 7..0	Timer 3 low byte 7...0 (only SPC 4-2 mode)
328_H		Error-Hi-Reg 15..8	Error counter register high byte 15...8 (only SPC4-2 mode) for error trigger signal
329_H		Error-Lo-Reg 7..0	Error register low byte 7...0 (SPC4-2 mode only)

Table 4-7 Assignment of the Internal Parameter Registers (Only for Read Access)

Address Intel/Motorola		Name	**Meaning** (write access !)
300_H	301_H	Int-Mask-Reg 7..0	Interrupt controller register
301_H	300_H	Int-Mask-Reg 15..8	
302_H	303_H	Int-Ack-Reg 7..0	
303_H	302_H	Int-Ack-Reg 15..8	
304_H	305_H	TSLOT 7..0	Settings for the wait-to-receive time
305_H	304_H	TSLOT 13..8	
306_H	307_H	BR-REG 7..0	Setting of the dividing factor
307_H	306_H	BR-REG 10..8	For generating the baud rate
308_H	309_H	TID1 7..0	
309_H	308_H	TID1 10..8	
$30A_H$	$30B_H$	FAKT-DEL-CLK 7..0	Delay timer for SM time service
$30B_H$	$30A_H$	FAKT-DEL-CLK 10..8	
$30C_H$- $30F_H$		reserved	
310_H		UMBR-PTR 7..0	UMBR-PTR points to the address of the first segment that **no longer** belongs to the indication queue.
311_H		Mode-Reg 7..0	Settings for individual bits
312_H		Mode-Reg1-Res 5..0	
313_H		Mode-Reg1-Set 5..0	
314_H		Base-PTR 7..0	Base address for access to the internal RAM
315_H		TRDY 7..0	Settings for TRDY (ready time valid before sending a reply frame)
316_H		PREAMBLE	Settings for the number of bits (preamble) in the synchronous mode.
317_H		TSYN	The following time is set: TSYN (33-bit asynchronous mode) TIFG (interframe GAP time; synchronous mode)
318_H		Mem-Lock 0	Memory lock cell
319_H		BEGIN-PTR 7..0	The BEGIN-PTR points to the lowest segment address of the indication queue. The BEGIN-PTR must always point to the beginning of an 8-byte segment.
$31A_H$		Mode-Reg2 7..0	Settings for individual bits
$31B_H$		Mode-Reg3 7..0	Settings for individual bits
$31C_H$		Mode-Reg4 7..0	Settings for individual bits (only SPC 4-2 mode)
$31D_H$		Timer-Typ-Reg 7..0	Mode setting time 0...3 (only SPC 4-2 mode)
$31E_H$		Timer-Control-Reg 7..0	Status control timer 0...3 (only SPC 4-2 mode)
$31F_H$		Clocked counter end value register 3..0	End value for counters of clocked frames (only SPC 4-2 mode)
320_H		Timer0-Reg 15..8	Timer 0 high byte 15...8 (only SPC 4-2 mode)
321_H		Timer0-Reg 7..0	Timer 0 low byte 7...0 (only SPC 4-2 mode)
322_H		Timer1-Reg 15..8	Timer 1 high byte 15...8 (only SPC 4-2 mode)
323_H		Timer1-Reg 7..0	Timer 1 low byte 7...0 (only SPC 4-2 mode)
324_H		Timer2-Reg 15..8	Timer 2 high byte 15...8 (only SPC 4-2 mode)
325_H		Timer2-Reg 7..0	Timer 2 low byte 7...0 (only SPC 4-2 mode)
326_H		Timer3-Reg 15..8	Timer 3 high byte 15...8 (only SPC 4-2 mode)
327_H		Timer3-Reg 7..0	Timer 3 low byte 7...0 (only SPC 4-2 mode)

Address Intel/Motorola	**Name**	**Meaning** (write access !)
328_H	Error-Hi-Reg 15..8	Writing to this register also deletes Error-Hi-Reg and Error-Lo-Reg
329_H	Error-Lo-Reg 7..0	Writing to this register also deletes Error-Hi-Reg and Error-Lo-Reg

Table 4-8 Assignment of the Internal Parameter Registers (Only for Write Access)

FLC Interface

5

5.1 SAP List

5.1.1 Structure of the SAP List

The SAP list is made up as follows:

- 5 SM-SAPs (System Management Service Access Point) each 5 bytes long
- DEFAULT-SAP (Service Access Point) with 16 bytes
  64 SAPs each 5 bytes long

Address	Name	register	Meaning
18H	SM1	Control Byte	Bit information
19H		Request-SA	Request source address
1AH		reserved	
1BH		reserved	
1CH		Reply-Update-Ptr/ SDN-DDB/-Tln-Tab-Ptr	Pointer to the reply buffer
1DH - 21H	SM2	analogous to SM1	analogous to SM1
22H - 26H	SM3	analogous to SM1	analogous to SM1
27H - 2BH	SM4	analogous to SM1	analogous to SM1
2CH - 30H	SM5	analogous to SM1	analogous to SM1
31H	DEFAULT SAP	Control byte	Bit information
32H		Request-SA	Request source address
33H		Request SSAP	Request source service access point
34H		Access-Byte	Access protection
35H		Reply-Update-Ptr/ SDN-DDB/-Tln-Tab-Ptr	Pointer to the reply buffer
36H		Reply-Update-Ptr D	
37H		Reply-Update-Ptr N	
38H		Reply-Update-Ptr U	
39H		Response-Buffer-Length	
3AH		Response Status	
3BH		Indication-Buffer-Ptr D	
3CH		Indication-Buffer-Ptr N	
3DH		Indication-Buffer-Ptr U	
3EH		Indication-Buffer-Length	
3FH		Active-Group-Ident	
40H		Control-Command	
41H	SAP[0]	Control byte	Bit information
42H		Request-SA	Request source address
43H		Request SSAP	
44H		Access-Byte	
45H		Reply-Update-Ptr/ SDN-DDB/-Tln-Tab-Ptr	Pointer to the reply buffer
46H - 4AH	SAP[1]	analogous to SAP [0]	analogous to SAP [0]
4BH - 17BH	SAP[2]- SAP[62]-	analogous to SAP [0]	analogous to SAP [0]
17CH	SAP[63]	Control byte	Bit information
17DH		Request-SA	Request source address
17EH		Request SSAP	
17FH		Access-Byte	
180H		Reply-Update-Ptr/ SDN-DDB/-Tln-Tab-Ptr	Pointer to the reply buffer

Table 5-1 SAP List

Service Access Points

In the FLC, a data transfer service is handled using a **Service Access Point, SAP)**. On each node, up to 64 SAPs are possible (SAP **[0..63]** and the DEFAULT SAP).

Communication between a DEFAULT SAP and a SAP is possible. The SPC 4-2 performs a validation of the request SSAPs.

Each service access point (including the DEFAULT SAP) has special entries in the SAP list with which the FLC provides receive resources. If the SPC 4-2 receives a frame a non-existent SAP, it replies with "no service activated" (SD1 response).

Individual registers are assigned to each SAP in the SAP list once this has been written.

5.1.2 Control Byte

Bit Position								Meaning
7	6	5	4	3	2	1	0	
SAP locked	SDN/ DDB filter	RS/RA or UE	RR	IN USE	Buffer available			Control byte

Bits 0-2	Buffer available These three bits are used as a counter for resources provided externally. The FLC increments the 3 bits as soon as a resource is available. The SPC 4-2 decrements the 3 bits when a received block was indicated. When it receives, the SPC 4-2 reads the 3 bits after it has received the complete frame. If the counter reading is zero, it aborts reception, sets the event flap 'No Resource' (RR, see below) and replies with no resource (SD1 response) **Exception:** If DP mode = 1 is set, buffer available is **not** changed by the SPC 4-2 in DEFAULT SAP. Buffer available must, however, be set to higher than zero otherwise the response will be no resource.
Bit 3	IN USE The SPC 4-2 sets this bit as soon as it has entered the complete frame of a request frame in the indication buffer. It resets it when an indication has been executed (valid or invalid). If the FLC wants to assign a new reply block, it must wait until the bit is reset. Only then can it reload the reply update pointer (under Mem-Lock). This prevents the FLC from reloading SPC 4-2 data when sending. **Exception:** If DP mode = 1 is set, the in-use bit is **not** set by the SPC 4-2 in the DEFAULT SAP. A correctly received request frame at the DEFAULT SAP is **not** entered in the indication queue and **not** indicated.
Bit 4	**RS/RA or UE** **No service activated/ Service access point blocked or user error:** the SPC 4-2 sets this flag when the validation of the request SA was negative (request SA does not match received SA; in other words the call comes from an unauthorized node). The SPC 4-2 replies with **Service Access Point Blocked [RA]** in the PA mode **or no service activated [RS]** in the PROFIBUS mode (SD1 response). This flag is also set when request SA = 7FH; in other words, the SAP is inactive. The SPC 4-2 replies with **No service activated [RS]** (SD1 response). This bit is set as a user error [UE] is the SAP was locked. The SPC 4-2 replies with **User Error [UE]** (SD1 response).
Bit 5	**RR = No Resource** The SPC 4-2 sets this bit if the content of the buffer available bits is zero after receiving the frame header; in other words, the FLC has not provided any resources or the queue is full. In both cases, the SPC 4-2 replies with **No Resource[RR]** (SD1 response).
Bit 6	**SDN-/DDB Filter** This bit allows the SDN-/DDB filter to be activated 0 = The "Reply-Update-Ptr/SDN-/DDB-Tln-Tab-Ptr" pointer points to the Reply-on-Indication-Block and therefore to the response to be sent. If the pointer = 00H, there is no response buffer and the SPC 4-2 replies with an SRD request with a short confirmation (SC). 1 = The "Reply-Update-Ptr/SDN-/DDB-Tln-Tab-Ptr" pointer points to the node table and the SPC 4-2 is "Subscriber" for this SAP. The SDN-/DDB-Tln list is evaluated during a "Subscriber for DDB-Response" access or SDN request.
Bit 7	**SAP locked** The SAP is not currently accepting data. If the SPC 4-2 receives data for this SAP, it sets the event flag user error (UE) and replies with user error (SD1 response).

Table 5-2 Control Byte

5.1.3 Request SA

Description

The received SA is compared with this entry. If it does not match, the SPC 4-2 sets the event flag no service activated (RS) and replies with service access point blocked [RA] in the PA mode and no service activated [RS] in the PROFIBUS mode (SD1 response). At the DEFAULT SAP, the addresses 00H - 7EH are possible, for all other SAPs 80H - FEH (extension bit set), where 7FH leads to 'No Service Activated' since 7Fh blocks the SAP. If this entry = FFH (= all), there is no validation of the call. On receiving an SRD with DDB, the "SDN-/DDB Filter" bit is tested and a further comparison is made in the DDB-TIn list before a response is sent or the event flag set.

5.1.4 Request SSAP

Description

The received SSAP is compared with this entry. If they do not match, the SPC 4-2 sets the event flag no service activated (RS) in the PA mode and service access point blocked (RA) in the PROFIBUS mode and replies with no service activated (SD1 response). If request SA is 00H-7EH, request SSAP = FFh selects the DEFAULT SAP. If the extension bit in the request SA is set and request SSAP = FFH, SSAP is not validated.

5.1.5 Access Byte

Description

The access byte controls the access protection to the corresponding SAP when receiving. If the entry is 0h, this means "No Access Protection". If the SPC 4-2 receives a frame that does not match the access byte, it replies with "NO SERVICE ACTIVATED". The RS event bit is set.

In the direction of the FLC, all access violations are filtered, the response [RS] (no service activated) is sent to the requester. **An exception to this is the case of a DDB response (subscriber), this is not acknowledged negatively.**

Bit Position								Meaning
7	6	5	4	3	2	1	0	
IND-U-Cleared	IND-N-Cleared	IND-N Valid	RUP-N Valid	Access Value				Access-Byte

Bit 0-3	Access Value Access Protection 0H = All 1H = SDN-Low 2H = SDN-High 3H = SDN-Low/High 4H = - 5H = SDA-Low 6H = SDA-High 7H = SDA-Low/High 8H = SRD-Low/High DDBREQ DDB-RES-Low/High 9H = SRD Low AH = SRD-High BH = SRD-Low/High CH = DDB-REQ DH = DDB-RES-low EH = DDB-RES-high FH = DDB RES low/high
Bit 4	RUP-N-Valid (only with DEFAULT-SAP) This bit is set by the application when valid input data are entered in the reply update buffer N. The SPC 4-2 resets RUP-N-Valid when it has swapped the reply update buffers D and N.
Bit 5	IND-N-Valid (only with DEFAULT-SAP) The SPC 4-2 sets this bit when valid output data are entered in the indication buffer N in the DP mode. The FLC resets IND-N-Valid when the FLC has swapped the indication buffers N and U.
Bit 6	IND-N-Cleared (only with DEFAULT-SAP) The "IND-N-Cleared" bit can only be evaluated when "IND-N-Valid = 1" is set. If "IND-N-Valid = 1" is set, then: 0 = The output data in indication buffer N can be adopted. 1 = The output data in indication buffer N must be replaced by the corresponding clear coding. The last received output data are entered in indication buffer N.
Bit 7	IND-U-Cleared (only with DEFAULT-SAP) The "IND-U-Cleared" bit must be set by the user on entering the fail-safe status and reset when the fail-safe status is exited. The SPC 4-2 does not modify this bit. The SPC 4-2 does, however, scan the bit when "Spec-Clear-Mode=1" is set and a "Read-Output-Data" frame is received in the DP mode. 0 = If the application is not in the fail-safe state; in other words the application uses the data of indication buffer U as the output data. If "Spec-Clear-Mode = 1" is set, the user must reset "IND-U-Cleared=0" to update the output data when "IND-N-Valid=1" and "IND-N-Cleared=0" are set. 1 = If the application is in the fail-safe state; in other words the application uses the clear coding as output data. The data in indication buffer U are then invalid. If "Spec-Clear-Mode = 1" is set, the user must set "IND-U-Cleared=1" to update the output data when "IND-N-Valid=1" and "IND-N-Cleared=1" are set.

Table 5-3 Access Byte

5.1.6 Reply-Update-Ptr/ SDN-/DDB-Tln-Tab-Ptr:

The "Reply-Update-Ptr/ SDN-/DDB-Tln-Tab-Ptr" pointer points to the indication reply buffer or to the SDN/DDB-Tln list (see also SDN-/DDB filter). The data buffers must be located above the UMBR-PTR in the SPC 4-2.

Structure

The structure of the SDN-/DDB-Tln list is described in the following table:

SDN-/DDB-Tln-List (Optional)		
tab-data-length	8 bits	Number of entries in the SDN-/DDB-Tln list. The physical length of the list is (n*2)+2 bytes for "n" entries
don't care	8 bits	
Request-SA 1	8 bits	First entry in the DDB-Tln list, meaning as for Request-SA
Request-SSAP 1	8 bits	First entry in the DDB-Tln list, meaning as for Request-SSAP.
.....		
Request-SA n	8 bits	nth entry in the DDB-Tln list, meaning as for Request-SA
Request-SSAP n	8 bits	nth entry in the DDB-Tln list, meaning as for Request-SSAP.

Table 5-4 : SDN-/DDB-Tln List

SDN Frames

All SDN frames (except for SM-TIME, that is always indicated) and DDB response frames can be filtered by the SPC 4-2 using the node table. The "Request-SA" and the "Request-SSAP" are defined in this node table per entry. An indication results only if the received SDN-/DDB frame is validated by one of the entries.

SDN Filter

The SDN-/DDB filter is active when the "SDN/DDB Filter" bit is set in the receive SAP. The node table is addressed using the "SDN-/DDB-Tln-Tab-Ptr" pointer. If "tab-data-length"=0, there is no validation of the SDN-/DDB-Tln list.

Sending over the Default SAP

To allow the sender to use the DEFAULT SAP, "req-ssap=0FFh" and the extension bit "req-sa"=0 must be entered in the node table at the receiving end. In all other cases, the extension bit "req-sa"=1 is set.

5.1.7 Special Features of the DEFAULT SAP

When using the DP mode, the following entries can also be processed in the SAP list.

- Reply-Update-Ptr D, N, U:
  These 8-bit pointers each point to the first segment of the reply update buffer D, N or U. The FLC collects the input data in the reply update U and then swaps the U buffer with the reply update N. The SPC 4-2 replies to a request frame with the input data of the reply update buffer D. The SPC 4-2 receives new input data by swapping the D and N buffers. The reply update buffers D, N or U contain only the net data.

- Response-Buffer-Length:
  This value specifies the length of the reply update buffers D, N and U (0 to 246 bytes).

- Response-Status:
  Specifies the priority of the response frames to the DP master. 2 values are permitted:

- 08_H: Response low priority

- $0A_H$: Response high priority

- Indication-Buffer-Ptr. D, N and U:
  These 8-bit pointers each point to the first segment of the indication buffers D, N or U.
  The SPC 4-2 enters error-free received output data from the DP master in indication buffer D and then swaps the D buffer with the indication buffer N (possibly only after Sync, see Section 2.7). The output data of the FLC are in the indication buffer U. The FLC obtains new output data by swapping indication buffers U and N. The indication buffers D, N or U contain only the net data.

- Indication-Buffer-Length:
  This value specifies the length of the indication buffers D, N or U (0 to 246 bytes).

- Active-Group-Ident:
  This byte encodes the membership of the DP slave in a maximum of 8 groups. The Active-Group-Ident is ANDed bit-by-bit with the Group-Select-Byte of a received global-control frame (GCT). The DP slave is addressed when the AND logic operation returns a value other than zero in at least one position. If the group-select byte of the GCT is zero, all DP slaves are addressed.

- Control-Command of a GCT:
  The last received control command of a global control frame is entered here by the SPC 4-2.

5.2 SM-SAP List

Structure of the SM-SAP Entries

The structure of the SM-SAP entries is analogous to those with normal SAPs.

Register	Meaning
Control Byte	Bit information
Request-SA	Request source address
reserved	
reserved	
Reply-Update-Ptr/SDN-DDB/-Tln-Tab-Ptr	Pointer to the reply buffer

Unnecessary SAPs should be deactivated, for example with Request-SA=7Fh.

SAP	Service	Transmission Function Code	Description
SM1	SM_SDN	2	SM-SDN frames
SM2	SM_SRD_SLOT_DEL	10	SM-SRD-Slot-Del frames
SM3	SM_SRD_SLOT_KEEP	11	SM-SRD-Slot-Keep frames
SM4	SM_SRD	1	SM-SRD frames
SM5	SM_Time	0	SM-Time frames

Table 5-5 : SM-SAP List

Usage

The use of the SM-SAPs depends on the control octet. No SAP extensions are used, analogous to the use of the DEFAULT SAP.

Based on the received frame (CO field), the SPC 4-2 recognizes which SM service is to be executed and automatically assigns it to the corresponding SAP (see table).

The SM_TIME and SM_SDN services are transferred to the indication queue like all other frames; no resources are required for sending (slave).

5.3 Indication Queue

5.3.1 Description

Function

If the SPC 4-2 receives a frame, it enters the frame header in the indication queue and **then** checks the free length in the queue (this is possible because one segment must always remain free). If at least one segment (8 or 16 bytes) is free (in addition to the special free segment), it continues reception and enters the data in the queue as long as there is free memory available. When a request frame (call) is received, the SPC 4-2 validates the frame header characters with the values it has set in the SAP list. The structure is described Table 5-1 SAP List.

The indication queue is managed as a ring buffer with read (IND-RD) and write (IND-WR) pointers. The SPC 4-2 is responsible for the write pointer and the FLC is responsible for the read pointer.

The IND-WR-PRE pointer allows fast slave reactions (e.g. for DP). With a suitable parameter assignment, an indication interrupt is generated after correct reception of the request frame and not at the end of the next frame to another node.

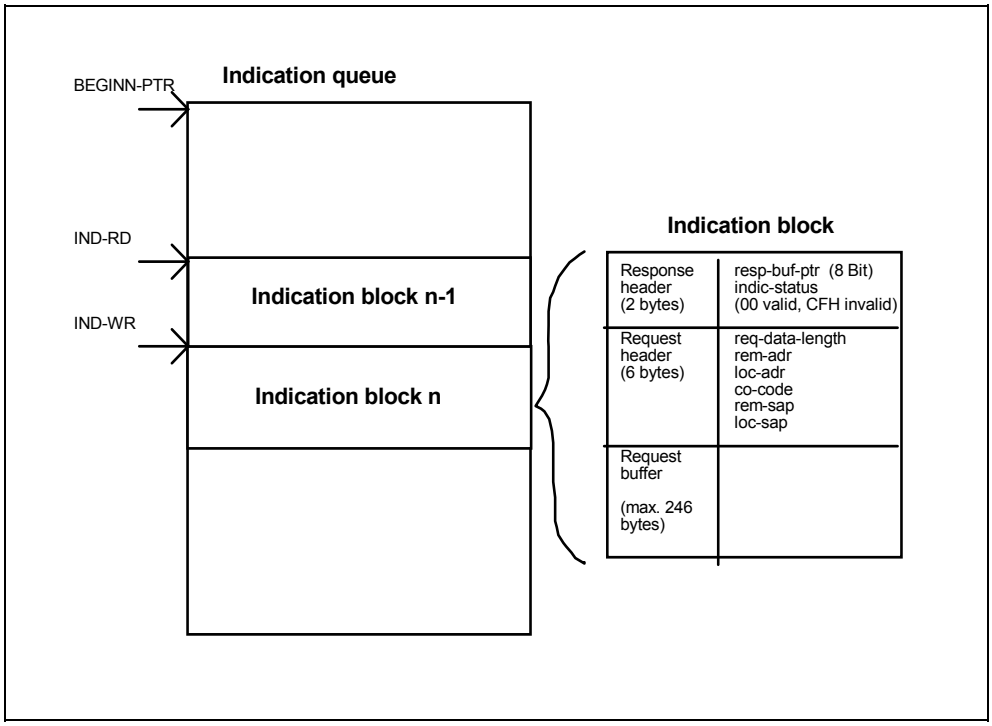

Figure 5-6 Structure of the Indication Queue

If a frame is received without a SAP extension (rem-SAP, loc-SAP), the SPC 4-2 enters 0FFh in the relevant cell.

If a frame is received without a SAP extension (rem-SAP, loc-SAP), the SPC 4-2 enters 0FFh in the relevant cell.

5.3.2 Structure of the Indication Block

	Response header		
Byte 0	resp-buf-ptr	This pointer points to the swapped-out response buffer (in the reply-on-indication-blocks area, refer to the memory area distribution). It is copied by the SPC 4-2 from the SAP list.	
Byte 1	indic-status	Here, the SPC 4-2 enters the status 00 for a 'valid indication'.	
	Request header (frame header characters of the requester)		
Byte 2	req-data-length	This value specifies the length of the net data entered in the request buffer (0 to 244 bytes with SAP extension, 0 to 246 bytes without SAP extension).	
Byte 3	rem-adr	Here, the SPC 4-2 enters the received SA. The remote node that will be involved in data exchange with the relevant service access point of the local station. It can be specified as a filter in req-sa in the SAP lists.	
Byte 4	loc-adr	Here, the SPC 4-2 enters the received DA.	
Byte 5	co-code	This value specifies the function code of the request frame. Here, the complete control octet is entered as received from the bus.	
		Function	Code
		Request FDL Status with Reply	x9h
		Send Data with no Acknowledge low	x4h
		Send Data with no Acknowledge high	x6h
		Send Data with Acknowledge low	x3h
		Send Data with Acknowledge high	x5h
		Send and Request Data low	xCh
		Send and Request Data high	xDh
		SM_Time	x0h
		SM_SRD	x1h
		SM_SDN	x2h
		SM_SRD_SLOT_DEL	xAh
		SM_SRD_SLOT_KEEP	xBh
		Send and Request Data with DDB	x7h
		DDB-Response low	y8h
		DDB-Response high	yAh
		x: Frame type 1 meaning bit 6=1 and FCB/FCV according to frame entry	
		y: Frame type 0 meaning bit 6=0 and station type[2] according to frame entry	
		Bit 7 (b8) of the received control octet is only evaluated for SM time frames, with all other request frames, bit 7 (b8) of the control octet is don't care.	
Byte 6	rem-sap	Here, the SPC 4-2 enters the service access point (SSAP) of the remote node. This field is only valid when the extension bit in rem-adr is set (the higher two bits of the rem-sap must be '0'). If a frame is received without a SAP extension (rem-SAP, loc-SAP) the SPC 4-2 enters 0FFh.	
Byte 7	loc-sap	Here, the SPC 4-2 enters the service access point (DSAP) of the local node. This field is valid only when the extension bit in rem-adr is set. If a frame is received without a SAP extension (rem-SAP, loc-SAP) the SPC 4-2 enters 0FFh.	
	Request buffer contains the received frame		
Byte 8	data 0	Byte 0 of the net data	
Byte 8+x	data 0+x	Byte x of the net data	

Table 5-7 : Indication Block

[2] Note: The station type with PROFIBUS DP is bit 5 (b6) and bit 4 (b5). With PROFIBUS PA, bit 7 (b8) is also relevant.

5.4 Reply-on-Indication Blocks

5.4.1 Description

Function

The FLC must provide the reply data in the buffers of the reply-on-indication blocks. If reply data are requested, the SPC 4-2 fetches the reply update pointer from the relevant SAP lists and sends the data from the reply buffer. Once the job is completed, the SPC 4-2 indicates the job by entering the status (valid indication) in the response header, setting the write pointer to the next free segment, and generating the IND interrupt.

A job is completed and indicated when:

- An SM frame, an SDN or a DDB response frame has been received free of error and validated.
- An SDA or SRD frame has been received error-free and validated, the response has been sent and the next request frame to another node or (with toggled FCB/FCV bits) to the local station address has been correctly received.

If the SPC 4-2 receives an SRD or DDB request frame with a net data length = 0 and if the response data length is also = 0, the SPC 4-2 does **not** enter this frame in the indication queue and does **not** indicate it (empty polling).

The FLC can control how often the data are sent from the indication reply buffer by setting a bit in the responder status (byte 2). If bit (4): single update reply is set in the "resp-status" of the indication reply buffer, a reply in the indication reply buffer is sent only once. If this bit = logical "0", the SPC 4-2 sends the buffer again (multiple update reply) with each call frame to this SAP.

The least significant nibble (lower 4 bits) specifies whether the job is sent with high or low priority.

5.4.2 Structure of the Reply-on-Indication Blocks

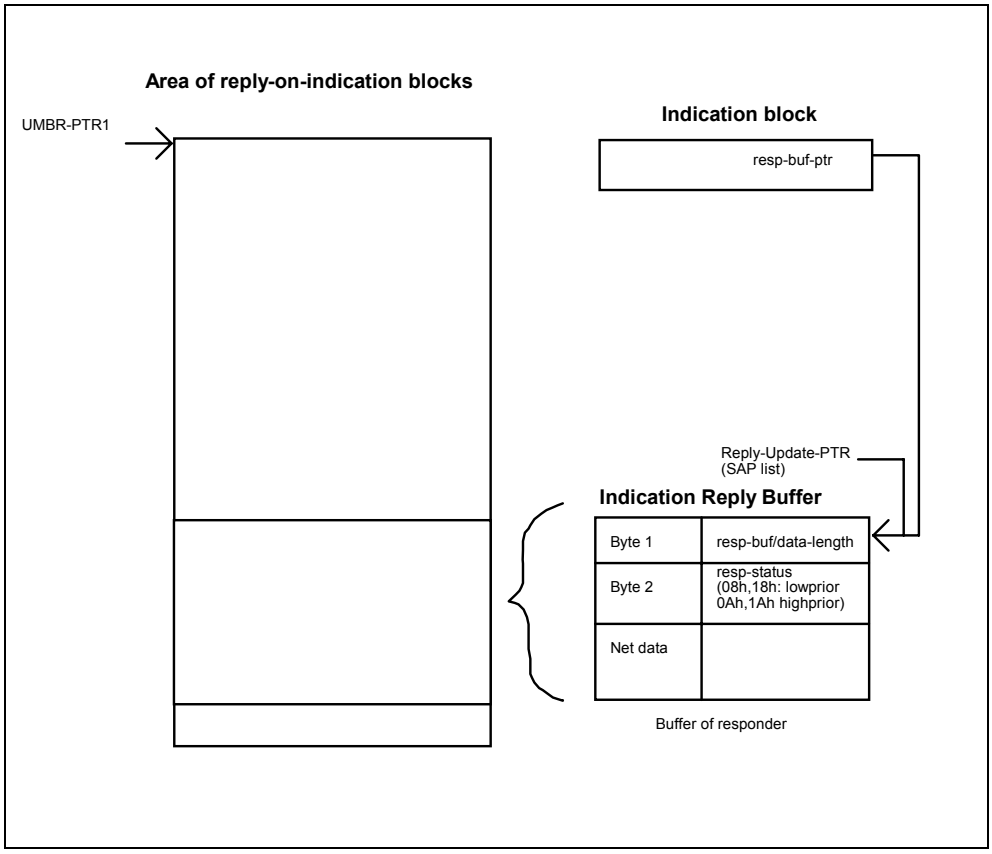

Figure 5-8 Structure of the Reply-on-Indication Block

The response buffer is included in the 'Reply-On-Indication Blocks' area and contains the response buffer length, the response status, and the net data of the response frame.

Reply Header			
Byte 0	resp-data-length	Here, the FLC enters the length of the response buffer.	
Byte 1	resp-status	The responder status is entered in this field. The status must be provided by the FLC. The following codes are permitted.	
		Function	Code
		Response FDL/FMA1/2-Data low	000x1000b
		(& Send Data okay)	
		Response FDL/FMA1/2-Data high	000x1010b
		(& Send Data okay)	
		Bit (4) = x :Single-Update-Reply	
		If this bit is also set, a reply in the indication reply buffer is sent only once. Otherwise, the SPC 4-2 sends this buffer again with each call frame.	
	Reply buffer contains the reply data		
Byte 3	data 0	Byte 0 of the net data	
Byte 8+x	data 0+x	Byte x of the net data	

Table 5-9 : Reply-On-Indication Block

DP Interface

6

6.1 Description

Supported Productive Services

The SPC 4-2 supports the following productive services of PROFIBUS DP (DIN 19245 part 3, EN 50170 volume 2, IEC 61158, IEC 61784-1)

- Data Exchange
- Read Input Data
- Read Output Data
- Global-Control (Sync, Freeze, Clear-Data)

Other DP Services

Other PROFIBUS-DP services (diagnostics, parameter assignment, and configuration) must be implemented by the FLC; in other words, the software must operate the appropriate SAPs according to the PROFIBUS DP state machine.

If the SPC 4-2 is to support the services above, DP mode = 1 must be set in mode register 0.

In the DP mode, the data exchange between the DEFAULT SAP of the DP master and the DEFAULT SAP of the DP slave is achieved using swap buffers:

The indication buffers D, N, and U are available for received data (output data). The reply update buffers D, N, and U are used for reply data (input data).

Interrupt

An indication interrupt is not generated. If new output data are available to the FLC, the "Output Data Exchange" interrupt is generated. The "Watchdog Reset" interrupt shows that valid output data have been received from the DP master at the DEFAULT SAP. The "Watchdog Reset" interrupt, instructs the FLC to reset the "Software Watchdog" that monitors the activity of the DP master.

Request frames at a SAP other than the DEFAULT SAP are accepted only if the SSAP is different from the DEFAULT SAP. The request SSAP must have suitable parameters assigned by the FLC. The received data are entered in the indication queue. As the reply, the data from the reply update buffer pointed to by the Reply-Update-Ptr of the addressed SAP are sent. If the received request data are entered in the indication queue, the "IND-WP-PRE" pointer is set to the next free segment and the "IND-PRE" interrupt is generated. If the job is completed, the IND-WP pointer is also set to the next free segment and the "IND" interrupt generated (indication).

Swap Buffer Principle

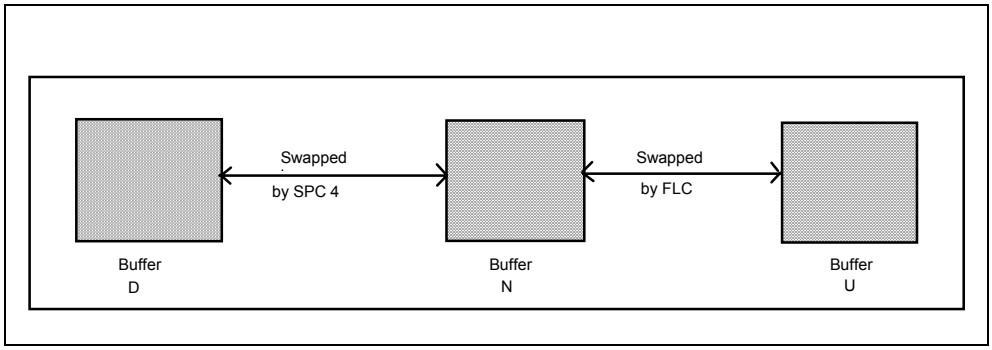

Figure 6-1 Swap Buffer Principle

The SPC 4-2 enters error-free output data received from the DEFAULT SAP of the DP master at the local DEFAULT SAP in the indication buffer D. The SPC 4-2 generates the "Watchdog Reset" interrupt. Following this, the SPC 4-2 swaps the indication buffers D and N either immediately (DIAG.SYNC mode = 0) or at the next "Sync" command (DIAG. SYSNC mode = 1). After swapping the indication buffer pointers D and N, the SPC 4-2 sets the IND-N-Valid = 1 flag in the default SAP and generates the "Output Data Exchange" interrupt. These actions are executed with the lock active to ensure data consistency. If the FLC wants to update its output data in the indication buffer U, it must first check whether IND-N-Valid = 1 is set (in other words, whether valid output data are entered in indication buffer N). If this is the case, the FLC can update its output data by swapping the indication buffers N and U. The FLC must also reset the flag IND-N-Valid = 0 in the DEFAULT SAP. These actions must be performed by the FLC with lock active.

The FLC puts together the input data in the reply update buffer U and then swaps the U buffer with the reply update buffer N.

The FLC must also set the flag RUP-N-Valid = 1 in the DEFAULT SAP if the reply update pointers U and N are swapped. These actions must be performed by the FLC with lock active. If the DP master requests input data using a request frame, the SPC 4-2 replies

- either with the "old" input data of reply update buffer D (in other words reply update buffers D and N are **not** swapped before sending the response). This is the situation when no valid input data have been entered in the reply update buffer N (in other words, RUP-N-Valid = 0 in the DEFAULT SAP) or the input data in reply update buffer D are frozen (DIAG.FREEZE mode = 1, see Section 6.2.4).

- or with the "new" input data if the reply update buffers D and N were swapped prior to sending the response. The buffers are swapped if RUP-N-Valid = 1 and DIAG. FREEZE mode = 0 is set. The SPC 4-2 then sets the flag RUP-N-Valid = 0 in the DEFAULT SAP. The buffers are swapped and the RUP-N-Valid flag is reset with lock active.

6.2 Productive Services

6.2.1 Data Exchange

Description

The controller for the PROFIBUS DP protocol must be implemented by the FLC. As a DP slave, the SPC 4-2 can only receive request frames from the DEFAULT SAP of the DP master at its own DEFAULT SAP when the DP controller is in the "Data Exchange" state. The FLC must therefore set

Request-SA = station address of the DP master

in the DEFAULT SAP. In all other DP states (for example Wait-PRM, Wait-Config), the DEFAULT SAP must be deactivated by the FLC with

Request-SA = 7FH

A request frame from the DP master at the DEFAULT SAP is then rejected with "No-Service-Activated (RS)".

In the DP mode, the following must be set in the DEFAULT SAP of the SPC 4-2:

Request SSAP = FFH (for DEFAULT-SAP)
Access-Value = 08H

Access-Value = 08H filters all request frames except for

- Send and Request Data low (SRD-low),
- Send and Request Data high (SRD-high),
- Send and Request Data with DDB (DDB-Request),
- DDB-Response low,
- DDB-Response high.

Since the filter allows DDB-Response-low/high frames to pass, this means that the SPC 4-2 as a DP slave can also listen on the bus using the DEFAULT SAP and evaluate the received data. Since the publisher is generally not the DP master, the SDN/DDB filter should be activated. If the SDN/DDB filter bit in the control byte of the DEFAULT SAP is set, the source address (SA) and SSAP are validated solely in the SDN/DDB node list. Received DDB response frames are entered in the indication queue. Following this, the "IND-WP-PRE" and "IND-WP" pointers are set to the next free segment and the "IND-PRE" and "IND" interrupts are generated.

If an SRD-low/high frame is received from the DP master and there are no input data present (in other words response buffer length = 0), the SPC 4-2 responds as follows:

- **either** with SC if 08H is entered in the response status of the DEFAULT SAP (in other words low priority).
- **or** with an SD2 frame with a length LE = 4 (in other words net data length = 1) if 0AH is entered in the response status of the DEFAULT SAP (in other words high priority). SPC4-1 and SPC4-2 send 00H as a dummy byte, with SPC4 this was FFH.

If a DDB request is received from the DP master and there are no input data available (in other words, response buffer length = 0), the SPC 4-2 responds with "No-Service-Activated (RS)" and sets the RS flag in the control byte of the DEFAULT SAP.

6.2.2 Read-Input-Data

Description

Read-Input-Data is an SRD frame without request data from any bus master with SSAP = 62 to SAP 56 of the DP slave. As a DP slave, the SPC 4-2 can only evaluate this frame if the DP controller is in the "Data Exchange" state. In all other states (for example Wait-PRM, Wait-Config), SAP 56 must be deactivated by the FLC with Request-SA = 7FH. A Read-Input-Data frame would then be rejected with "No-Service-Activated (RS)".

In the "Data Exchange" DP status, the following settings must be made in SAP 56 of the SPC 4-2:

Buffer-available > 0
Request-SA = FFH (all)
Request-SSAP = SSAP (different from DEFAULT-SAP)
Access-Value = {09H, 0AH, 0BH}
Reply-Update-Ptr / SDN-/DDB-Tln-Tab-Ptr = don't care

Read-Input-Data frames are **not** indicated by the SPC 4-2 and **not** entered in the indication queue. Buffer available is **not** decremented in the control byte of SAP 56. .

If input data are requested with Read-Input-Data, the SPC 4-2 replies as follows:

- **either** with the "old" input data of reply update buffer D (in other words reply update buffers D and N are **not** swapped before sending the response).

- This is the situation when no valid input data have been entered in the reply update buffer N (in other words, RUP-N-Valid = 0 in the DEFAULT SAP) or the input data in reply update buffer D are frozen (DIAG.FREEZE mode = 1, see Section 2.7.4).

- **or** with the "new" input data if the reply update buffers D and N were swapped prior to sending the response. The buffers are swapped if RUP-N-Valid = 1 and DIAG, FREEZE mode = 0 are set in the DEFAULT SAP. The SPC 4-2 then sets the flag RUP-N-Valid = 0 in the DEFAULT SAP. The buffers are swapped and the RUP-N-Valid flag is reset with lock active.

  If Response-Buffer-Length = 0 is set in the DEFAULT SAP, the SPC 4-2 replies with SC.

  An SRD frame with request data at SAP 56 of the DP slave is rejected by the SPC 4-2 with "No-Resource (RR)".

6.2.3 Read-Output-Data

Description

Read-Output-Data is an SRD frame without request data from any bus master with SSAP =62 to SAP 57 of the DP slave. As a DP slave, the SPC 4-2 can only evaluate this frame if the DP controller is in the "Data Exchange" state. In all other states (for example Wait-PRM, Wait-Config), SAP 57 must be deactivated by the FLC with Request-SA = 7FH. A Read-Output-Data frame would then be rejected with "No-Service-Activated (RS)".

In the "Data Exchange" DP status, the following settings must be made in SAP 57 of the SPC 4-2:

Buffer-available > 0
Request-SA = 0FFH (all)
Request-SSAP = SSAP (different from DEFAULT-SAP)
Access-Value= {09H, 0AH, 0BH}
Reply-Update-Ptr / SDN-/DDB-Tln-Tab-Ptr = don't care

Read-Output-Data frames are **not** indicated by the SPC 4-2 and **not** entered in the indication queue. Buffer available is **not** decremented in the control byte of SAP 57. .

Read-Output-Data causes the SPC 4-2 to reply with the output data of indication buffer U.

If Indication-Buffer-Length = 0 is set in the DEFAULT SAP, the SPC 4-2 replies with SC.

An SRD frame with request data at SAP 57 of the DP slave is rejected by the SPC 4-2 with "No-Resource (RR)".

6.2.4 Global Control (Sync, Freeze, Clear Data)

Description

The global control frame is an SDN frame with 2 bytes of net data from the DP master with SSAP = 62 to SAP 58 of the DP slave. As a DP slave, the SPC 4-2 can only evaluate this frame if the DP controller is in the "Data Exchange" state. In all other states (for example Wait-PRM, Wait-Config), SAP 58 must be deactivated by the FLC with Request-SA = 7FH. A Global-Control frame (GCT) would then be rejected with "No-Service-Activated (RS)".

In the "Data Exchange" DP status, the following settings must be made in SAP 58 of the SPC 4-2:

Buffer-available > 0
Request-SA = Station address of DP master
Request-SSAP = SSAP (different from DEFAULT-SAP)
Access-Value = {01H, 02H, 03H}
Reply-Update-Ptr / SDN-/DDB-Tln-Tab-Ptr = don't care

Buffer available is **not** decremented in the control byte of SAP 58. . A global control frame with a net data length other than 2 is not evaluated by the SPC 4-2 if "Check-GCT-Length-Off = 0" is set in mode register 2.

If "Check-GCT-Length-Off = 1" is set, monitoring of the net data length of a global control frame is deactivated.

The global control function allows a special control command to be sent to one (single), several (multi), or all (broadcast) DP slaves. The data format of the two data bytes is shown in the table below.

Address	Bit Position								Meaning
	7	6	5	4	3	2	1	0	
Byte 0	Res	Res	Sync	Unsync	Freeze	Unfreeze	Clear_Data	Res	Control-Command
Byte 1	Select7	Select6	Select5	Select4	Select3	Select2	Select1	Select0	Group-Select

Byte 0: Control Command

Bit	Meaning	Meaning
0	Reserved	"Reserved" indicates that these bits are reserved for future expansions and must have the value "logical 0". If the bit "Check-GCT-Resbits-Off = 0" is set in mode register 2, the reserved bits are scanned for zero. If at least one of the reserved bits has the value "logical 1", the SPC 4-2 executes "Leave-Master". If "Check-GCT-Resbits-Off = 1" is set, the reserved bits for the SPC 4-2 are "don't care".
1	Clear_Data	Output data in the indication buffer are deleted and the Output_Data_Exchange interrupt is generated.
2	Unfreeze	If unfreeze is set, the SPC 4-2 deactivates the freeze mode (DIAG.FREEZE mode = 0) and swaps the reply update buffers D and N if the flag RUP-N-Valid = 1 is set in the DEFAULT SAP. The SPC 4-2 then sets RUP-N-Valid = 0. These actions are executed with lock active. If "DIAG.FREEZE-Mode = 0" is set, the SPC 4-2 replies to a request frame requesting input data with the "new" input data (in other words, the SPC 4-2 swaps the reply update buffers D and N prior to sending the response if the flag RUP-N-Valid = 1 is set in the DEFAULT SAP).
3	Freeze	If freeze is set, the SPC 4-2 activates the freeze mode (DIAG.FREEZE mode = 1) and swaps the reply update buffers D and N if the flag RUP-N-Valid = 1 is set in the DEFAULT SAP. The SPC 4-2 then sets RUP-N-Valid = 0. The SPC 4-2 executes these actions with lock active. If input data are requested from the SPC 4-2 with a request frame in the freeze mode, the SPC 4-2 responds with the "old" input data of reply update buffer D (in other words, reply update buffers D and N are **not** swapped prior to sending the response.
4	Unsync	If unsync is set, the SPC 4-2 deactivates the sync mode (DIAG.SYNC mode = 0) and swaps the indication buffers D and N if valid data are entered in the D buffer. It also sets the IND-N-Valid = 1 flag in the DEFAULT SAP and generates the "Output-Data-Exchange" interrupt. If DIAG. SYNC mode = 0 is set when a global control frame with unsync = 1 is received, unsync has no effect. If DIAG.SYNC mode = 0, the SPC 4-2 swaps the indication buffers D and N immediately when it receives new valid output data.
5	Sync	If sync is set, the SPC 4-2 activates the sync mode (DIAG.SYNC mode = 1), without swapping the indication buffers D and N. If DIAG.SYNC mode = 1 is set when a global control frame with sync = 1 is received, the SPC 4-2 swaps the indication buffers D and N if the D buffer contains valid output data. It also sets the IND-N-Valid = 1 flag in the DEFAULT SAP and generates the "Output-Data-Exchange" interrupt. The SPC 4-2 executes these actions with lock active. If DIAG.SYNC mode = 1 is set, the SPC 4-2 enters new output data from the DP master in indication buffer D and generates the "Watchdog-Reset" interrupt. The SPC 4-2, however, waits until the next "Sync" command before swapping the indication buffers D and N.
6,7	Reserved	see bit 0

Table 6-2 : Global Control

Byte 1: Group Select

Group select decides which groups of DP slaves will be addressed.

The bits of the group select byte of a received global control frame are ANDed by the SPC 4-2 with the bits of the "Active-Group-Ident" byte of the DEFAULT SAP. The DP slave is addressed when the AND logic operation returns a value other than zero in at least one position.

If the group-select byte is 00H, all DP slaves are addressed. If the control command of a global control frame (GCT) does **not** match the control command in the DEFAULT SAP, the SPC 4-2 enters the GCT in the indication queue and generates the indication interrupt. The received control command is also stored in the DEFAULT SAP.

6.2.5 Leave-Master

Description

With "Leave-Master", the SPC 4-2 executes the following actions:

- Output data in indication buffer D are deleted, or more precisely, written with 00H.
- Following this, indication buffers D and N are swapped (with lock active).
- The "Control-Command" byte in the default SAP is deleted (in other words, Control-Command :=FFH)
- The "Output-Data-Exchange" interrupt is **not** generated
- DEFAULT SAP, SAP 56, SAP 57, SAP 58 are deactivated; in other words, Request-SA = 7FH is entered in all 4 SAPs with lock active.
- Generates the "Leave-Master" interrupt.

The SPC 4-2 executes "Leave-Master" in the following situations:

- The "Cmd-Leave-Master = 1" bit is set in mode register 1:
- At the end of "Leave-Master", the SPC 4-2 sets "Cmd-Leave-Master" back to "logical 0" in mode register 1.
- At least 1 reserved bit is "logical 1" in the control command of a GCT and "Check-GCT-Resbits-Off = 0" is set in mode register 2.

- The received net data length of a DP data frame is **less than** the indication buffer length in the DEFAULT SAP:
  The SPC 4-2 replies with the input data from reply update buffer D, if DIAG.FREEZE mode = 0 and RUP-N-Valid = 1, the reply update buffers D and N are first swapped.

- The received net data length of a DP data frame is **greater than** the indication buffer length in the DEFAULT SAP:
  The SPC 4-2 replies with "No-Resource (RR)" and sets the RR flag in the control byte of the DEFAULT SAP to "logical 1".

The execution time t_{LM} required by the SPC 4-2 for "Leave-Master" depends on the indication buffer length n and the baud rate:

- 12 Mbauds: (25 + n) bit clocks < t_{LM} < (30 + 1.5 n) bit clocks

- For baud rates ≤3 Mbauds : tLM ≈ (20 + n/2) bit clocks

Notice:

With "Leave-Master", there is a risk that request frames received at the SPC 4-2 during the execution time t_{LM} are lost. Since the receiver of the SPC 4-2 is operational during the time t_{LM} but cannot be processed, a "FIFO-Overflow" interrupt is possible.

6.2.6 Baudrate Search

Description

If the "Baudrate-Search" bit is set in mode register 1, the automatic baud rate search function is active. In this mode, the SPC 4-2 does not evaluate the frames and simply checks whether or not a frame was received physically error free or not. To be able to receive reply frames as well, T_{SYN} is reduced to 10 bit times regardless of the value set in the SYN-Time register. If the received frame is bad, the "Wrong-SD" interrupt is generated. If SD4 or a complete SD1/SD2/SD3 frame is received error free, the "Correct-SD" interrupt is generated. An SC received free of errors is ignored.

The baud rate to be checked must be set by the FLC.

ASIC Interface 7

Overview

The following sections describe the registers that specify both the hardware function of the ASIC and the frame processing.

Parameters that intervene directly in the controller or semaphores that are set directly by the controller are stored in a parameter latch array on the SPC 4-2. All other parameters are in the lower area of the RAM. The FLC transfers operating data to the SPC 4-2 in the parameter cells. Parameters are set only in the offline status (for example after turning on). All parameters must be loaded before the SPC 4-2 can leave the offline status (START-SPC 4-2 = 1, mode register 1). Some control bits must, however, be modified continuously during operation. These are put together in a special register (mode register 1) and can be set or cleared independent of each other.

7.1 Latch Parameters

7.1.1 Slot-Time Register

(can be written, modifiable only in offline status):

Address	Bit Position								Meaning
Control register	7	6	5	4	3	2	1	0	
304_H (Intel)	TS L7	TS L6	TS L5	TS L4	TS L3	TS L2	TS L1	TS L0	TSLOT 7..0

Address	Bit Position								Meaning
Control register	15	14	13	12	11	10	7	8	
305_H (Intel)			TS L1 3	TS L 12	TS L 11	TS L 10	TS L 9	TS L8	TSLOT 13..8

Table 7-1 : Slot Time Register

The wait to receive time TSL is a maximum of 14 bits long and is specified in transmission bit steps. It is required to calculate the timeout.

7.1.2 Baudrate Register

(can be written, modifiable only in offline status):

Address	Bit Position								Meaning
Control register	7	6	5	4	3	2	1	0	
306_H (Intel)	BR7	BR6	BR5	BR4	BR3	BR2	BR1	BR0	BR-Reg 7..0

Address	Bit Position								Meaning
Control register	15	14	13	12	11	10	7	8	
307_H (Intel)						BR 10	BR 9	BR8	BR-REG 10..8

Table 7-2 : Baudrate Register

The dividing factor for the baud rate generator is set in the baud rate register. The dividing factor G is calculated according to the following formula:

$$G = \frac{CLK}{BR * ABTAST} - 1$$

CLK = clock in MHz
BR = baudrate
G = dividing factor

ABTAST is obtained from the FILTER-AN/AUS and SYN/ASYN bits of mode register 0:

SYN/ASYN	FILTER-AN/AUS	ABTAST
0	0	16
0	1	16
1	0	4
1	1	16

The following table lists the dividing factors for the individual baud rates for both modes:

CLK	Baudrate (BR)	Dividing factor (G) for ABTAST = 4	Dividing factor (G) for ABTAST = 16
48 MHz	12.0 MBd	0	-
48 MHz	6.0 Mbd	1	
48 MHz	3.0 Mbd	3	0
48 MHz	1.5 Mbd	7	1
48 MHz	500.00 kbd	23	5
48 MHz	187.50 kbd	63	15
48 MHz	93.75 kbd	127	31
48 MHz	45.45 kbd	263	65
48 MHz	31.25 kbd	383	95
48 MHz	19.2 kbd	624	-
48 MHz	9.6 kbd	1249	-

Table 7-3 : Dividing Factors

7.1.3 BEGIN-PTR Register

(can be written, modifiable only in offline status):

Address	Bit Position								Meaning
Control register	7	6	5	4	3	2	1	0	
319_H	BPTR7	BPTR6	BPTR5	BPTR4	BPTR3	BPTR2	BPTR1	BPTR0	BEGIN-PTR 7..0

Table 7-4 : BEGIN-PTR Register

The BEGIN-PTR is the address of the first segment of the indication queue.

7.1.4 UMBR-PTR Register

(can be written, modifiable only in offline status):

Address	Bit Position								Meaning
Control register	7	6	5	4	3	2	1	0	
310_H	UPTR7	UPTR6	UPTR5	UPTR4	UPTR3	UPTR2	UPTR1	UPTR0	UMBR-PTR-Reg 7..0

Table 7-5 : UMBR-PTR Register

The UMBR-PTR points to the address of the first segment that **no longer** belongs to the indication queue.

7.1.5 BASE-PTR Register

(can be written):

Address	Bit Position								Meaning
Control register	7	6	5	4	3	2	1	0	
314_H	BASE-PTR7	BASE-PTR6	BASE-PTR5	BASE-PTR4	BASE-PTR3	BASE-PTR2	BASE-PTR1	BASE-PTR0	BASE-PTR-Reg 7..0

Table 7-6 : BASE-PTR Register

The base pointer addresses the beginning of the 256-byte memory window.

7.1.6 TRDY Register

(can be written):

Address	Bit Position								Meaning
Control register	7	6	5	4	3	2	1	0	
315_H (Intel)	TRDY 7	TRDY 6	TRDY 5	TRDY 4	TRDY 3	TRDY 2	TRDY 1	TRDY 0	TRDY-Reg 7..0

Table 7-7 : TRDY Register

The TRDY time must elapse as an idle time on the bus before a response frame is sent. It is a maximum of 8 bits long and is specified in transmission bit steps.

The FLC can change TRDY if the MAC state machine is **not** in the offline status.

In the DP mode, TRDY can be modified dynamically by the DP master sending the DP slave a parameter assignment frame with the new value of TRDY. Since the SPC 4-2 does not evaluate parameter assignment frames, this must be handled by the FLC. The value for TRDY to be set by the FLC is obtained as follows:

TRDY for SPC 4-2 = T_{RDY} from the parameter assignment frame + 2.

7.1.7 PREAMBLE Register

(can be written, modifiable only in offline status):

Address	Bit Position								Meaning
Control register	7	6	5	4	3	2	1	0	
316_H (Intel)							PREAB1	PREAB0	PREAMBLE 7..0

Table 7-8 : PREAMBLE Register

PREAB: number of pREAMBLE bytes
- 00 = 1
- 01 = 2
- 10 = 4
- 11 = 8

In the synchronous mode of the serial interface, the number of pREAMBLE bytes can be set here.

7.1.8 SYN-Time Register

(can be written, modifiable only in offline status):

Address	Bit Position								Meaning
Control register	7	6	5	4	3	2	1	0	
317_H (Intel)			TSYN 5	TSYN 4	TSYN 3	TSYN 2	TSYN 1	TSYN 0	TSYN-Reg 7..0

Table 7-9 : SYN-Time Register

In the asynchronous mode (RS-485), 33 bits must always be set here.

In the synchronous mode, the T_{IFG} (interframe GAP time) is set (4...32 bits)

7.1.9 Delay-Timer Register

(can be read)

Address	Bit Position								Meaning
Control register	7	6	5	4	3	2	1	0	
306_H (Intel)	TDEL 7	TDEL 6	TDEL 5	TDEL 4	TDEL 3	TDEL 2	TDEL 1	TDEL 0	DELAY 7..0

Address	Bit Position								Meaning
Control register	15	14	13	12	11	10	7	8	
307_H (Intel)	TDEL 15	TDEL 14	TDEL 13	TDEL 12	TDEL 11	TDEL 10	TDEL 9	TDEL 8	DELAY 15..8

Table 7-10 : Faktor-Delay-Timer-Clock-Reg

The Delay-Timer Register register contains the current counter reading of the delay timer.

7.1.10 Factor-Delay-Timer-Clock Register

(can be written):

Address	Bit Position								Meaning
Control register	7	6	5	4	3	2	1	0	
$30A_H$ (Intel)	TFAK 7	TFAK 6	TFAK 5	TFAK 4	TFAK 3	TFAK 2	TFAK 1	TFAK 0	TFAKOT 7..0

Address	Bit Position								Meaning
Control register	15	14	13	12	11	10	7	8	
$30B_H$ (Intel)						TFAK 10	TFAK 9	TFAK 8	TSLOT 13..8

Table 7-11 : Factor-Delay-Timer-Clock Register

The Factor-Delay-Timer-Clock register determines the dividing factor dependent on the input clock pulse for the delay timer (refer to the section on SPC 4-2 timers).

7.1.11 Mode Register

Mode Register 0

Mode-REG0, can be written, modifiable only in offline status): Fixed parameters are transferred to mode register 0 that only need to be loaded once (following a reset):

Address	Bit Position								Meaning
Control register	7	6	5	4	3	2	1	0	
311_H	FILTER_AN /AUS	EARLY-READY	INT-POL	XPB/PA	XRTS/ADD	SYN/ASYN	DP Mode	DIS-START-CONTROL	Mode-Reg0 7..0

Bit 0 DIS-START-CONTROL

Disable start bit monitoring (hamming distance 4, test in UART)

0 = Start bit monitoring is enabled in the receiver (status following reset)

1 = Start bit monitoring is disabled in the receiver

Bit 1 DP-Mode

Set DP mode

0 = No DP functions are supported (status following reset)

1 = The following productive services are supported:

- Data-Exchange
- Read-Input-Data
- Read-Output-Data
- Global-Control frame (Sync, Freeze, Clear-Data)

Bit 2 SYN/ASYN

Switchover bit for synchronous or asynchronous mode on the serial interface

0 = Synchronous mode (status following reset)

1 = Asynchronous mode

Bit 3 XRTS/ADD

XRTS/ADD output switchover for different driver activation

0 = RTS (status following reset)

1 = ADD

Bit 4 XPB/PA

Layer 2 setting

0 = PROFIBUS mode (status following reset)

1 = PA Mode

Bit 5 INT-POL

Polarity of the interrupt outputs

0 = The interrupt outputs are low active (status following reset)

1 = The interrupt outputs are high active

Bit 6 EARLY-RDY

Early ready signal

0 = Ready is generated when the data is valid (read) or when the data is accepted (write).(status following reset)

1 = Ready is brought forward by one clock pulse

Bit 7 FILTER_AN/AUS

Activate receive filter

0 = Filter deactivated (status following reset)

1 = Filter activated

Caution:

If the filter is active during asynchronous transmission, this reduces the maximum baud rate from qclk-in/4 to qclk-in/16 (example: 48 MHz/4 = 12 Mbauds or 48 MHz/16 =3 Mbauds).

Table 7-12 : Mode Register 0

Mode Register 1

(Can be written, START-SPC 4-2, modifiable only in offline status; EOI, SM-MODE can be modified during operation)

Some control bits must, however, be modified continuously during operation. These are put together in a special register (mode register 1) and can be set (Mode_Reg_S) or cleared (Mode_Reg_R) independent of each other. Different addresses are used for setting and clearing. A logical '1' must be written to the bit position to be set or cleared.

Address	Bit Position								Meaning
Control register	7	6	5	4	3	2	1	0	
312_H			Baudrate Search	DEL-TIM		SM-Mode			Mode-Reg1-Reset 7..0
313_H		Cmd-Leave-Master	Baudrate Search	DEL-TIM	Go-Offline	SM-Mode	EOI	START SPC 4-2	Mode-Reg1-Set 7..0

Bit 0 **START-SPC 4-2**

Exit the offline status

1 = The SPC 4-2 leaves the online status and changes to passive idle or the SM mode depending on whether the SM mode bit was also set and the idle and syni timers are started.

Bit 1 **EOI**

End of Interrupt

1 = End of Interrupt, the SPC 4-2 switches the interrupt outputs inactive and sets EOI back to logical '0'.

Bit 2 **SM Mode**

SM Mode

1 = If this bit and START-SPC 4-2 are set, the SPC 4-2 changes to the SM mode state The SPC4-2 accepts only SM frames in the SM-Mode-State.

Bit 3 **Go-Offline**

Go to the offline state

1 = Once the current job is completed, the SPC 4-2 changes to the offline state

Bit 4 **DEL-TIM**

Delay timer

1 = The delay timer is stopped (SET) or reset (RESET)

Bit 5 **Baudrate Search**

Automatic baud rate search

1 = Automatic baud rate search is activated:

If SD4 or a complete SD1/SD2/SD3 frame is received error free, the "Correct-SD" interrupt is generated. An SC received free of errors is ignored.

If the received frame is bad, the "Wrong-SD" interrupt is generated.

Bit 6 **Cmd-Leave-Master**

This is evaluated only if DP mode = 1 is set in mode register 0.

1 = Output data in indication buffer D are deleted, or more precisely, written with 00H.

Indication buffers D and N are swapped.

The following SAPs are locked with Request-SA = 7FH:

- DEFAULT-SAP (for Data-Exchange)
- SAP-38 (for Read-Input-Data)
- SAP-39 (for Read-Output-Data)
- SAP-3A (for Global Control Frame)

"Leave-Master" interrupt is generated and Cmd-Leave-Master = 0 is reset

Table 7-13 : PREAMBLE Register

Mode Register 2

Mode register 2 of the SPC 4 was extended by three bits (7..5) in the SPC 4-1 and therefore also in the SPC 4-2:

Mode register 2 (can only be written)

Address	**Bit Position**								**Meaning**
Control register	7	6	5	4	3	2	1	0	
$31A_H$	EN-DD B-MO DE	EN-CLOC K-SYNC	SPEC - CLEA R-MOD E	CHECK-GCT-RESBIT S-OFF	CHECK-GCT-LENGTH-OFF	X86	XINT CI	XHOL DTOK EN	Mode-Reg2 7..0

Bit 0	XHOLDTOKEN Here, the level of the output pin XHOLDTOKEN can be set. This output exists only to ensure pin compatibility with SPC2. 0 = Low 1 = High (reset value)
Bit 1	XINTCI Here, the level of the output pin XINTCI can be set. This output exists only to ensure pin compatibility with SPC2. 0 = Low 1 = High (reset value)
Bit 2	X86 This bit only influences the asynchronous Intel mode 0 = If this bit is cleared, access is started with the falling edge of ALE and access is therefore only possible when ALE = 0. This allows an extremely fast series of accesses, for example for 80C165 1 = Following a reset, it has value 1 and disables the ALE input (in other words the level at this pin is immaterial). The SPC 4-2 is therefore in the X86 mode and access is started by edges at XRD/XWR.
Bit 3	Check-GCT-Length-Off Check the frame length of a global control frame 0 = The length of a global control frame is monitored, if this is not 2, the GCT is ignored 1 = No monitoring of the data length
Bit 4	Check-GCT-Resbits Off Check the reserved bits of a global control frame 0 = The reserved bits in the command byte of a global control frame are monitored. 1 = No monitoring of the reserved bits in the command byte of a global control frame. If at least one of these reserved bits is logical 1, the SPC 4-2 executes a "Leave-Master".
Bit 5	SPEC-CLEAR-MODE In the Spec_Clear_Mode (fail-safe mode), the SPC 4-2 accepts data frames with a net data length of 0 when the PROFIBUS master is in the clear mode. 0 = Fail-safe mode off 1 = Fail-safe mode enabled
Bit 6	EN-CLOCK-SYNC (time-of-day synchronization) XPB/PA = 0 (PROFIBUS mode): 0 = No time-of-day synchronization (status following reset); in other words, SM2-Time0/1 frames are filtered 1 = Time-of-day synchronization is active for several time masters XPB/PA = 1 (PA mode): 0 = Time-of-day synchronization of the SPC 4 is set. 1 = Time-of-day synchronization is active for several time masters
Bit 7	EN-DDB-MODE XPB/PA = 0 (PROFIBUS mode): 0 = All DDB frames are filtered (status following reset). 1 = DDB is enabled XPB/PA = 1 (PA mode): Status of EN-DDB-MODE unimportant, DDB mode is always enabled.

Table 7-14 : Mode Register 2

The extension of mode register 2 in the SPC 4-1 and SPC4-2 is compatible with the SPC 4 in terms of software since the current server software sets bits 5 to 7 of the data bus to 0 when it makes the parameter settings in this register.

Mode Register 3

Mode register 3 (can only be written)

Address	Bit Position								Meaning
Control register	7	6	5	4	3	2	1	0	
$31B_H$	FF Mode	RXD level	XHOLDTOKEN Mode		Segment 16	Quick-Sync-New	Debug	Pulse modulation	Mode-Reg3 7..0

Bit 0	Pulse Modulation
	Pulse modulation for the current-saving link between SPC4-1 or SPC4-2 and the ASIC SIM1 can be activated here.
	0 = Pulse modulation is deactivated (reset value)
	1 = Pulse modulation is enabled
Bit 1	Debug
	The SPC4-1 or SPC4-2 triggers an interrupt (write violation) as soon as a previously specified micro sequencer command is executed.
	0 = Debug interrupt disabled (reset value)
	1 = Debug interrupt enabled
Bit 2	Quick-Sync-New
	Activates the improved fast synchronizer in the Manchester receiver
	0 = Improvement is inactive (reset value)
	1 = Improvement active
Bit 3	Segment16
	Activates the 16 byte segments for addressing of the 3K RAM of the SPC4-2
	0 = 8 byte segments (reset value)
	1 = 16-byte segments; in other words, complete addressing of the 3K RAM is possible.
Bit 5..4	XHOLDTOKEN Mode
	Function of the output pin XHOLDTOKEN
	00 = After reset; XHOLDTOKEN function as for SPC4/SPC4-1 (see mode register 2)
	01 = Error trigger signal on receive error, pulse
	10 = Error trigger signal on send error compare with level at TXD_TXS, pulse
	11 = Error trigger signal on send error compare with level at RXD_RXS, pulse
Bit 6	RXD_RXS level
	RXD_RXS level for XHOLDTOKEN mode "11"
	0 = No inversion compared with TXD_TXS (reset value)
	1 = The send signal is inverted on the way from TXD_TXS to RXD_RXS.
Bit 7	FF Mode
	Activates the FF mode (see Section 7.7)
	0 = No FF mode (reset value)
	1= FF mode active

Table 7-15 : Mode Register 3

Mode Register 4

Mode register 4 is new in the SPC 4-2 and contains the following bits:

Address	Bit Position								Meaning
Control register	7	6	5	4	3	2	1	0	
$31C_H$	Enable-SPC 4-2				Sampling mode	Enable-Takt-Sync		Start_FF-Send	Mode-Reg4 7..0

Bit 0	Start-FF-Send
	Start for sending a frame (only possible in FF mode)
	0 = Sending deactivated (reset value)
	1 = The SPC 4-2 starts to send a frame immediately unless it is currently receiving. It then sends the frame when it has finished receiving. This is only possible when the FF mode bit is active in mode register 3.
Bit 1	Enable-Takt-Sync
	Clock synchronization
	0 = Reset value
	1 = The SPC 4-2 reacts to global control frames.
Bit 3..2	Sampling mode
	Size of the unsharp window for pulse demodulation
	00 = Unsharp window 2.5µs to 3.0µs as for the SPC 4-1
	01 = Unsharp window 3.0 µs to 3.5 µs (reset value)
	10 = Unsharp window 3.5µs to 4.0µs
	11 = Unsharp window 4.0µs to 4.5µs
Bit 7	Enable-SPC 4-2
	Enable SPC4-2 enhancements
	0 = Status following reset. Reading the version number in the status register returns version number "01" of the SPC 4-1. When reading the parameter register, the SPC 4-2 does not evaluate address bits 7 to 5 (like the SPC4/SPC4-1).
	1 = When the version number is read, the SPC 4-2 returns the version number "10".

Table 7-16 : Mode Register 4

7.1.12 Status Register

The status register reflects the current SPC 4-2 status and can only be read.

Address	Bit Position								Meaning
Control register	7	6	5	4	3	2	1	0	
304_H (Intel)	Enable - Receiver	MEM - LOCK	EARLY - READY	IND-PRE Stored	IND-Stored	Passive-Idle	SM-state	OFF LINE	Status-Reg 7..0

Address	Bit Position								Meaning
Control register	15	14	13	12	11	10	9	8	
305_H (Intel)	Chip		Version		Stn-Typ	Idlemux		SYNI -/ XSLOT	Status-Reg 15 .. 8
	0	1	x	x		1	0		

x x Version number differs depending on setting of bit 7 in mode 4 register

0 1 Operation in SPC4-1 mode

1 0 Operation in SPC4-2 mode

Bit 0	Offline/Passive-Idle
	Offline-/Passive-Idle state
	0 = The SPC 4-2 is offline
	1 = The SPC 4-2 is passive-idle
Bit 1	SM-State
	SM state
	0 = The SPC 4-2 is not in the SM mode
	1 = The SPC 4-2 is in the SM mode
Bit 2	Passive-Idle
	Passive-idle state
	0 = The SPC 4-2 is not in the passive-idle state
	1 = The SPC 4-2 is in the passive-idle state
Bit 3	IND-Stored
	Indication temporarily stored
	0 = No indication temporarily stored
	1 = One indication temporarily stored
Bit 4	IND-PRE-Stored
	IND-PRE interrupt mode activated
	0 = An indication will be generated at the beginning of the next frame (no repetition)
	1 = An indication will be generated early (directly after error-free reception)
Bit 5	EARLY-READY
	Early ready signal
	0 = Ready is generated when the data are valid
	1 = Ready is generated one clock pulse before the data are valid
Bit 6	MEM-LOCK
	Bus access locked
	0 = No MEM-LOCK set
	1 = The processor has set MEM-LOCK
Bit 7	Enable-Receiver
	Enables the receiver
	0 = The receiver is disabled
	1 = The receiver is enabled
Bit 8	SYNI-/XSLOT
	State of the SYNI/Slot timer
	0 = The timer runs as a SLOT timer
	1 = The timer runs as a SYNI timer
Bit 9,	Idle-Mux1..0:
10	Status of the idle multiplexer
	00 = The Idle-Mux is set to TSYN
	01 = The Idle-Mux is set to baud rate search
	10 = The Idle-Mux is set to TID1
	11 = The Idle-Mux is set to TRDY
Bit 11	Stn-Typ
	Station type
	0 = Passive node

	1 =	Node in SM mode
Bit 12,	Version	
13	Version ID of the SPC 4-2	
	01 =	Version ID in the compatibility mode (as for SPC4-1)
	10 =	Version ID for SPC 4-2 extended mode
	Rest	Not possible
Bit 14,	Chip	
15	Coding	
	01 =	This code stands for the SPC 4-1 and SPC 4-2
	Rest	Not possible

Table 7-17 : Status Register

7.2 Fail-safe Mode

An additional mode register bit "Spec-Clear-Mode" (bit 5 in mode register 2), enables the fail-safe mode. The fail-safe mode is enabled by setting "Spec-Clear-Mode = 1".

The "IND-N-Cleared" and "IND-U-Cleared" bits are added to the access byte of the default SAP:

Access byte(3..0) := Access-Value
Access byte (4) := RUP-N-Valid
Access byte (5) := IND-N-Valid
Access byte (6) := IND-N-Cleared
Access byte (7) := IND-U-Cleared

Bit Position								Meaning
7	6	5	4	3	2	1	0	
IND-U-Cleared	IND-N-Cleared	IND-N Valid	RUP-N Valid	Access Value				Access-Byte

Bits 0-3	Access value
Bit 4	RUP-N-Valid (only with DEFAULT-SAP)
Bit 5	IND-N-Valid (only with DEFAULT-SAP)
Bit 6	IND-N-Cleared (only with DEFAULT-SAP) The "IND-N-Cleared" bit can only be evaluated when "IND-N-Valid = 1" is set. If "IND-N-Valid = 1" is set, then: The output data in indication buffer N can be adopted. The output data in indication buffer N must be replaced by the corresponding clear coding. The last received output data are entered in indication buffer N.
Bit 7	IND-U-Cleared (only with DEFAULT-SAP) The "IND-U-Cleared" bit must be set by the user on entering the fail-safe status and reset when the fail-safe status is exited. The SPC 4-2 does not modify this bit. The SPC 4-2 does, however, scan the bit when "Spec-Clear-Mode=1" is set and a "Read-Output-Data" frame is received in the DP mode. If the application is not in the fail-safe state; in other words the application uses the data of indication buffer U as the output data. If "Spec-Clear-Mode = 1" is set, the user must reset "IND-U-Cleared=0" to update the output data when "IND-N-Valid=1" and "IND-N-Cleared=0" are set. If the application is in the fail-safe state; in other words the application uses the clear coding as output data. The data in indication buffer U are then invalid. If "Spec-Clear-Mode = 1" is set, the user must set "IND-U-Cleared=1" to update the output data when "IND-N-Valid=1" and "IND-N-Cleared=1" are set.

Table 7-18 : Fail-safe Mode

If "Spec-Clear-Mode = 1" is set, the SPC 4-2 also accepts data frames without output data in the "Data Exchange" state of the DP controller. This applies regardless of the value of the indication buffer length set in the default SAP of the SPC 4-2. If "Spec-Clear-Mode = 1" is set, the SPC 4-2 performs the following actions after receiving a frame with a net data length = 0 (even if the selected indication buffer length > 0):

- Generates "Watch-Dog-Reset" interrupt.
- Generates the "Output-Data-Exchange" interrupt.
- Replies with input data.
- Sets IND-N-Valid := 1 and IND-N-Cleared := 1

If the user updates the output data by swapping indication buffers N and U, "IND-N-Valid = 1" and "IND-N-Cleared = 1" indicate that the output data must be replaced by the corresponding clear coding. The data received as a subscriber from DDB response frames that are located in the indication queue must also be replaced by the corresponding clear coding. In the clear state, the output data are not deleted by the SPC 4-2; in other words not overwritten by 00H.

If the SPC 4-2 receives a "Read-Output-Data" frame, it checks the "IND-U-Cleared" bit. If "IND-U-Cleared=1" is set, the SPC 4-2 replies with 00H as the output data.

With the "Spec-Clear-Mode = 1" setting, the SPC 4-2 does not delete the output data even when it executes Leave-Master or when it receives a global control frame with "Clear-Data = 1". To indicate the clear state, the SPC 4-2 sets "IND-N-Valid = 1" and "IND-N-Cleared = 1".

If "Spec_Clear_Mode = 0" is set, the SPC 4-2 behaves like the SPC 4. Fail-safe frames are not detected; in the clear state, the output data are overwritten with 00H. IND-N-Cleared is not set. IND-U-Cleared is don't care.

Notice:

The execution time t_{CLR} required by the SPC 4-2 to clear the output data depends on the indication buffer length "n" and the baud rate:
At 12 Mbauds this is approximately (15 + n) bit clocks < t_{CLR} < (20 + 1.5n) bit clocks.
For baud rates lower than 3 Mbauds it is approximately t_{CLR} = (20 + 0.5n) bit clocks.
This means that the SPC 4-2 requires approximately 150 bit clocks to clear 256 bytes at 31.25 kbauds. Since the bus parameter T_{ID1} (= 37 bit clocks) is significantly shorter at this baud rate, request frames to the SPC 4-2 can be lost.

7.3 Time-of-Day Synchronization

The SPC 4-2 supports two time-of-day synchronization mechanisms. The "En-Clock-Sync" parameter bit (bit 6 in mode register 2) selects the required mechanism.

If "En-Clock-Sync := 0" is set (status following reset), the SPC 4-2 behaves like the SPC 4 in terms of time-of-day synchronization. Time-of-day synchronization is then available only in the PA mode (XPB/PA = 1). In the PROFIBUS mode (XPB/PA = 0), the SM2-Time0/1 frames are filtered by the SPC 4-2. This mode should therefore no longer be used.

If "En-Clock-Sync := 1" is set, the SPC 4-2 supports a time-of-day synchronization mechanism that also permits the operation of several time masters. This mechanism is available both in the PA mode and in the PROFIBUS mode.

The delay timer integrated in the SPC 4-2 has been extended to 24 bits (SPC 4: 16 bit delay timer). Each overrun of the integrated delay timer causes a "Del-Tim-Overrun" interrupt (= bit 4 of the interrupt register) on the SPC 4-2 (as was also the case on the SPC 4). This interrupt allows the user to extend the internal delay timer as required.

To ensure compatibility with SPC 4, the delay timer of the SPC 4-2 is limited to 16 bits in the PA mode (XPB/PA = 1); in other words, the "Del-Tim-Overrun" interrupt is generated when the 16-bit timer overruns.

In the PROFIBUS mode (XPB/PA = 0) the delay timer is 24 bits wide. The "Del-Tim-Overrun" interrupt is generated when the 24-bit timer overruns. Bits 23 to 16 of the delay timer can be read out at address 310H.

The time base of the delay timer is 32 us on the SPC 4. The "Factor-Delay-Timer-Clock" parameter register determines the dividing factor for the delay timer. This allows any other time base to be set. To achieve a higher resolution in time-of-day synchronization, a time base of 1 us as well as 32 us is in discussion. The following dividing factors must then be set:

Quartz	Fakt-Del-CLK	Resolution
48 MHz	1535	32 us
20 MHz	639	32 us
2 MHz	63	32 us
48 MHz	47	1 us
20 MHz	19	1 us
2 MHz	1	1 us

7.4 DDB Mechanism

The DDB mechanism is enabled in the PROFIBUS mode (XPB/PA = 0) of the SPC 4-2 with "En-DDB-Mode := 1" (bit 7 in mode register 2). If this bit is not set, all DDB frames are filtered.

In the PA mode (XPB/PA = 1) of the SPC 4-2, the DDB mechanism is always enabled, the parameter bit "En-DDB mode" is of no significance in this mode.

With the SPC4/4-1 and SPC 4-2, the DDB mechanism is restricted to the default SAP. No other SAPs can be operated with DDB. The default SAP is the only SAP that provides separate resources for the SDN/DDB node table and for reply data (reply update buffers D, N, U) in the DP mode. If DP-Mode = 0 is set, either the node table for filtering SDN or DDB response frames or a Reply-on-Indication buffer for reply data is available to the SAPs even the default SAP.

7.5 Activating the Extensions

The expansions of the SPC 4-2 are all activated using previously unused parameter registers. The SPC4/SPC4-1 does not evaluate address bits 7 to 5 when the parameter registers are accessed so that all registers can be accessed under several addresses (write and read). This applies to both writing and reading. All SPC4/SPC4-1 registers and 4 new SPC 4-2 registers are located in the accessible address space from 0x300 to 0x31F. One of these is the new Mode4 register (see Section 7.1.11). If the Bit Enable-SPC 4-2 is activated here, the SPC 4-2 evaluates all address bits. This means that genuine access to addresses beyond 0x31F is possible where there are more new registers of the SPC 4-2.

If Enable-SPC 4-2 is not active, reading the version register returns version "SPC 4-1".

7.6 Memory Expansion to 3 Kbytes

The SPC 4-2 has an extra mode (can be set in mode register 3, see Section 7.1.11), in which the memory segment size of the internal RAM is increased from 8 to 16 bytes. With this mode, access to this RAM using the base pointer can theoretically address up to 4 Kbytes instead of the previous maximum of 2 Kbytes (although only 3 Kbytes are implemented.

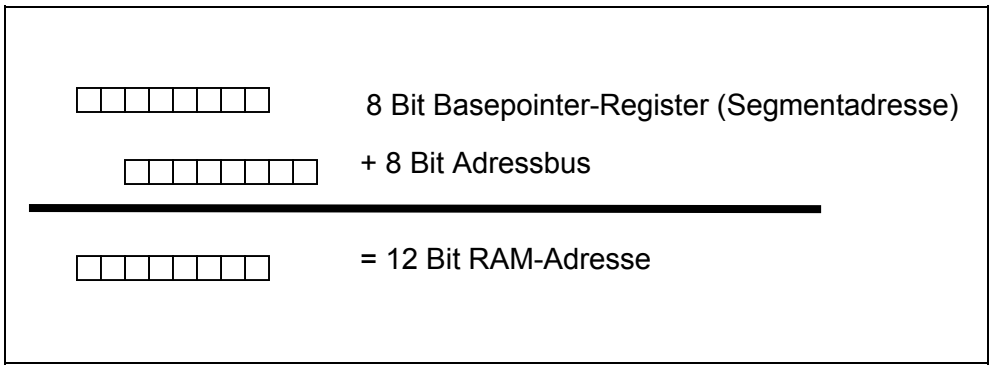

Figure 7-19 Memory Expansion to 3 Kbytes

When accessing data structures in this RAM in the new mode, it is therefore vital to know how the data is shifted when there is a change to the 16-byte segment size. The following rules apply to individual data structures:Data structures with 16 byte segments

- **SAP List:**
  On the SPC4/SPC4-1 as well as on the SPC 4-2, this area begins at address 24 (018_h). The SAP list is therefore not structured segment-oriented; in other words, the bytes of all 64 SAPs follow on one after the other without gaps. This structure was selected because this memory area of the internal RAM can be accessed directly without needing to use a base pointer.

- **Indication blocks:**
  Each indication block begins at a segment boundary. Before the data, it contains the response header and the request header making up a total of 8 bytes. The actual data are located in the next free segment. As a result, when using 16 byte segments on the SPC 4-2, there is a gap of 8 bytes between the headers and the data that follows. The data itself is stored without gaps.

- **Reply-On-Indication blocks:**
  Each of these blocks must begin at a segment boundary. In addition to the data, each of these blocks begins with 2 bytes of header information. In contrast to the indication blocks, the data follow on without a gap.

7.6.1 Memory Wastage with 16-Byte Segments

Due to the extra 16-byte segment for the 8-byte long header, each indication block wastes 8 bytes of memory. At the end of the data, in contrast to 8-byte segmentation, it can waste a further 8 bytes.

Each Reply-on-Indication block can waste a further 8 bytes at the end.

With an indication queue with space for 2 frames and 20 Reply-On-Indication blocks, the maximum possible wastage is 2*16 + 20*8 = 192 bytes.

7.6.2 Mem-Overflow Interrupt with 16-Byte Segments

The Mem-Overflow interrupt becomes active with 8-byte segments as soon as there is an attempt to access beyond the 2-Kbyte boundary.

The Mem-Overflow interrupt becomes active with 16-byte segments as soon as there is an attempt to access beyond the 3-Kbyte boundary.

7.7 FF Mode

After activating the FF mode with the FF-Mode bit of mode register 3 (the FF mode is a variant of the PA mode but does not work in the PA mode !), the user must activate the Start-SPC4 bit in mode register 1 as was the case on the SPC4/SPC4-1. The microprogram of the SPC 4-2 then changes to a state in which it waits for an FF send job for a received FF. The only way out of this state is to reset the SPC 4-2. The SPC 4-2 has one buffer for sending and one for receiving in the internal RAM.

7.7.1 Send and Receive Buffer Structure

Each buffer begins with 2 bytes of length information. The lower-order byte is located in the first byte of the buffer and the higher-order byte with the frame length is located in the second byte. These are followed by the data (caution: if a frame has 10 bytes of data, the length word in the send buffer also has the value 10, in the receive buffer, however, the value 12 is entered since this includes the two received CRC bytes). The buffers must begin at a segment boundary, although they themselves are byte-oriented; in other words, they never have gaps regardless of the segment size.

7.7.2 Sending

The user can trigger sending by writing a 1 to the Start-FF-Send bit in mode register 4. The SPC 4-2 6 then requires 6 bit times before the frame starts on the bus. If the Start-FF-Send bit is activated while reception is still active, there is a frame gap of 23 bit times on the bus. Half bit time after the end of the transmitted frame the SPC 4-2 activates the MAC_Reset interrupt, after a further bit time, it opens its receiver. The user must store the start address of the send buffer as a segment number in the IND_RD pointer.

7.7.3 Receiving

The user stores the start address of the receive buffer once again as a segment number in the IND_WP_PRE RAM memory location. The user defines the end of the receive buffer using the highest permitted segment number in the IND_WP RAM memory location.

If the microprogram attempts to write to the memory area that does not belong to the receive buffer, writing is suppressed although reception continues.

When a valid start delimiter is received, the and CORRECT_SD interrupt becomes active. This interrupt is therefore used for carrier detection.

If errors occur when the Manchester receiver is receiving, it can no longer reliably detect the end delimiter and therefore the end of the frame. Reception could then go on forever. To prevent this, reception is terminated by the microprogram whenever an error is detected during reception. If a CRC error occurs (detected in the last data byte), the two following CRC bytes are stored in the receive memory, whereas if a data bit error occurs (Manchester violation), the bad data byte ends up as the last or next to last in the receive memory (depending on how full the internal receive FIFO is). In either case, the length bytes indicate which byte was stored last in the receive buffer regardless of whether it was a CRC or data byte.

When reception is finished, the SPC 4-2 enters the received length in the length bytes of the receive buffer and activates the "frame received error-free" interrupt if no errors were detected during reception. If an error occurred, the "bad frame received" interrupt is activated. In this case, the user can decide whether this is a CRC error (station type = 1) or a Manchester error (station type = 0) based on bit 11 of the status register (station type).

If there was receive buffer overflow, and the received data were lost, the length information contains the correct length information but the receive buffer is filled only up to its defined end (there are less bytes in the receive buffer than indicated by the length bytes!). In this case, the "receive buffer overflow" interrupt is activated (when there is a receive buffer overflow, it is not possible to find out whether the frame was received with or without errors).

The SPC 4-2 activates the relevant interrupt approximately 17 bit times after the end of the frame. In the meantime, it empties the three-level FIFO of the Manchester receiver and updates the length bytes.

7.8 Error Trigger Signal

This signal should be used to trigger an oscilloscope if a transmission error occurs. It should be activated either by receive or send errors. A receive error means that the SPC 4-2 receiver detected an error in the bit stream. A send error means that the frame sent by the SPC 4-2 differs from the simultaneously received frame. The error trigger signal is led out via the XHOLDTOKEN pin, is zero-active, and in all cases has a minimum width of 1/4 bit time (except in operation with pulse modulation where the minimum width is the pulse width).

Receive errors:

Both in the PA and in the DP mode, the error bit of each character is used (in the PROFIBUS PA or FF mode, these are Manchester bit errors, in the PROFIBUS DP mode, start bit, parity, stop bit errors). This bit is updated after each character is received. In the PA mode, the CRC error signal, that can only be active once at the end of a frame while a frame is being received, is also checked. In the DP mode, the same applies to the checksum error signal. A FIFO overflow also counts as a receive error.

Send errors:

The send pin of the SPC 4-2 is bi-directional; in other words, the SPC 4-2 can check which level is supplied to its TXD_TXS send pin when sending. Instead of this level, it can also check using the value supplied by the RXD_RXS input pin.

This means that there are four different modes for the SPC 4-2 XHOLDTOKEN pin:

0. Normal operation as with the SPC 4-1

1. Error trigger signal for reception

2. Error trigger signal for sending (comparison with the level at TXD_TXS)

3. Error trigger signal for sending (comparison with the normal or inverted level at RXD_RXS; can be set with the RXD_RXS level bit of mode register 3); in this case, the external propagation time from the TXD_TXS send pin to the local RXD_RXS receive pin must be taken into account; depending on the mode, there is an upper limit for this value:

4.

PROFIBUS DP:	1 bit time
PROFIBUS PA/FF mode without pulse modulation:	0.5 bit times
PROFIBUS PA/FF mode with pulse modulation:	1 period of QCLK_IN

The active mode is set with the XHOLDTOKEN mode bits of mode register 3.

Error counter:

The error counter is a new SPC 4-2 16-bit register. It must be read by the host in bytes (high byte address 0x328, low byte address 0x329); in other words, word access is not allowed (no automatic swapping between "high" and "low" byte with Intel or Motorola access).

The counter reading is incremented each time the error trigger signal is activated. Once the counter reading FFFF is reached, the counter stops and must be deleted by the host by writing to the higher or lower byte. The data written has no significance, writing to the counter always deletes all 16 bits at the same time.

To ensure that the higher byte always matches the lower byte when reading out the error counter via the 8-bit data bus (consistency of the 16-bit value), the user must always read the lower byte first and then the higher byte (the mechanism is the same as for timers 0 to 3).

7.9 Interrupt Controller

The interrupt controller informs the processor (uP) of indication messages and various error events. Up to 16 events are stored on the interrupt controller and applied to an interrupt output. The controller has no priority level and does not supply an interrupt vector (not 8259A compatible!).

It consists of an interrupt request register (IRR), interrupt mask register (IMR), interrupt register (IR) and interrupt acknowledge register (IAR).

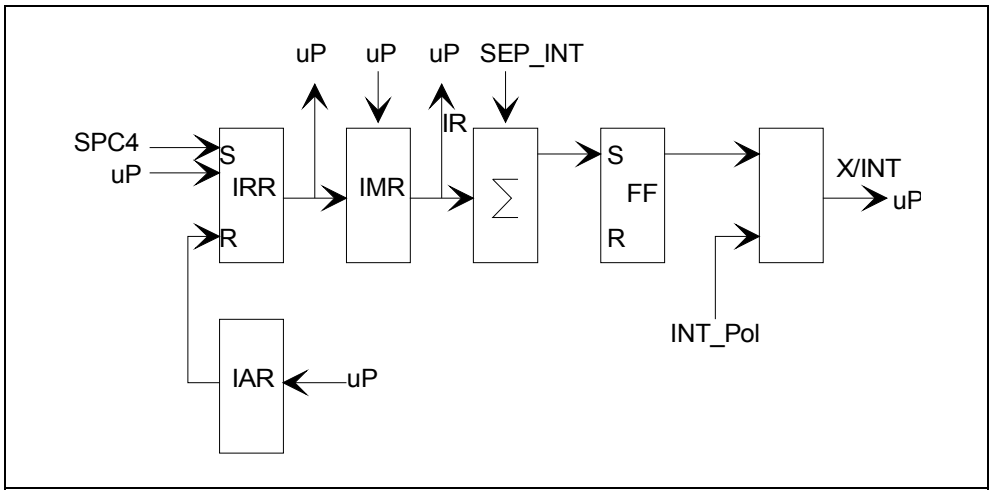

Figure 7-20 Interrupt Controller

Every event is stored in the IRR. Individual events can be suppressed using the IMR. The entry in the IRR does not depend on the interrupt mask. The event signals that are not masked in the IMR generate the X/INT interrupt over a common network. When debugging, the user can set every event in the IRR.

Every interrupt event processed by the processor must be deleted using the IAR by writing logical '1' to the corresponding bit position. If there is a new event and acknowledge pending in the IRR at the same time, the event remains stored. If the processor then enables a mask, make sure that there is no entry from the past in the IRR. To be on the safe side, the position in the IRR should be deleted before the mask is enabled.

Before exiting the interrupt routine, the processor must set the "End of Interrupt Signal (EOI) in mode register 1. This edge change switches the interrupt line inactive. If an event is still stored, the interrupt output only becomes active following an interrupt inactivity time of at least 48 clock periods (in other words, at 48 MHz = 1 usec). This makes it possible to return to the interrupt routine when using an edge-triggered interrupt input.

The polarity of the interrupt output can be set with the INT_Pol mode bit. After the hardware reset, the output is low active.

7.9.1 Interrupt Assignment

Address	**Bit Position**								**Meaning**
Control register	7	6	5	4	3	2	1	0	
302_H (Intel)	Correct -SD/ Output-Data-Exchange	Wrong SD/ Watch-Dog-Reset	Syni-Error	Del-Tim-Overrun	Go-Passive Idle	Go-SM-State	Rec-Frame Overflow	MAC_Reset	Int-Reg (IR) 7..0

Address	**Bit Position**								**Meaning**
Control register	15	14	13	12	11	10	9	8	
303_H (Intel)	IND	IND-PRE	FIFO overflow	Reserved	Leave-Master	Write-Violation	timeout	Mem-Overflow	Int-Reg (IR) 15..8

Bit 0	MAC_Reset
	After the SPC 4-2 has processed the current job, it changes to the offline state (by setting 'Go-Offline' or if a fatal error has occurred from SM mode).
Bit 1	REC-Frame-Overflow
	The SPC 4-2 received a new frame although the indication queue was still full or the FIFO in the UART had an overrun due to the processor locking the bus too long.
Bit 2	Go-SM-State
	The SPC 4-2 changed to the SM mode state.
Bit 3	Go-Passive-Idle
	The SPC 4-2 changed to the Passive-Idle state.
Bit 4	Del-Tim-Overrun
	The delay timer has overrun. This interrupt allows the FLC to extend the internal delay timer (24 or 16 bits) as necessary.
Bit 5	Syni-Error
	The Syni timer has elapsed.
Bit 6	Wrong-SD /Watch-Dog-Reset Wrong-SD: When baud rate search = 1; Bad reception with the baud rate search active Watch-Dog-Reset: When baud rate search = 0 and DP mode = 1: Valid data was received from the DP master.
Bit 7	Correct-SD / Output-Data-Exchange: Correct-SD: When baud rate search = 1; When no error occurred receiving a frame and baud rate search was active. Output-Data-Exchange: When baud rate search = 0 and DP mode = 1 Indication buffers D and N were swapped. DP data frame without output data (in other words, with net data length = 0) was received.
Bit 8	Mem-Overflow
	Access was attempted to the internal RAM at an address outside the 1.5 Kbytes.
Bit 9	timeout
	A timeout occurred. No further action on the SPC 4-2
Bit 10	Write-Violation
	Internal parameter cells in the RAM were overwritten externally, the SPC 4-2 changes to the offline state.
Bit 11	Leave-Master
	The SPC 4-2 leaves the PROFIBUS DP Data_Exchange state
Bit 12	Ignore_Delay-Timer-Overrun
	With the SM2 time slave controller in the W-T1 state, an SM2-Time0 frame was received from the current time master. This interrupt is always masked in the PA mode.
Bit 13	FIFO overflow
	The internal FIFO has overflowed. Reception of frames was stopped.
Bit 14	IND-PRE
	The SPC 4-2 has detected a premature indication.
Bit 15	IND
	The SPC 4-2 has executed an indication.

Table 7-21 : Interrupt Register

7.9.2 Interrupt Assignment in the FF Mode

As soon as the FF mode is activated, the interrupt sources are switched over.

The bits are of these 16-bit interrupt register have the following meaning in the FF mode:

Address	Bit Position								Meaning
Control register	7	6	5	4	3	2	1	0	
302_H (Intel)	Corr ect-SD	Time r 3	Syni-Error	Time r 2	Time r 1	Time r 0	Rec-Frame Overflo w	MAC – Rese t	Int-Reg (IR) 7..0

Address	Bit Position								Meaning
Control register	15	14	13	12	11	10	9	8	
303_H (Intel)	IND	Rese rved	FIFO overfl ow	Rese rved	Rese rved	Write - Viola tion	Reserv ed	Mem - Overf low	Int-Reg (IR) 15..8

The other registers of the interrupt controller have the same bit positions as the IR:

Address	register		Reset state	Assignment	
300_H / 301_H	Interrupt-Request-Register (IRR)	Read only			
300_H / 301_H	Interrupt-Mask register (IMR)	can be written, can be modified in operation	all bits deleted	Bit = 1 Bit = 0	Mask is set and the interrupt disabled. Mask is deleted and the interrupt enabled.
302_H / 303_H	Interrupt-Acknowledge-Register (IAR)	can be written, can be modified in operation	all bits deleted	Bit = 1 Bit = 0	The IRR bit is deleted. The IRR bit remains unchanged.

Table 7-22 : Further Interrupt Registers

Bit 0	MAC_Reset
	Frame sent
Bit 1	Rec-Frame Overflow
	Receive buffer overflow
Bit 2	Timer 0
	Timer 0 elapsed
Bit 3	Timer 1
	Timer 1 elapsed
Bit 4	Timer 2
	Timer 2 elapsed
Bit 5	Syni-Error
	Error receiving frame (CRC or Manchester error)
Bit 6	Timer 3
	Timer 3 elapsed
Bit 7	Correct-SD
	Correct start delimiter received
Bit 8	Mem-Overflow
	Access was attempted to the internal RAM at an address outside the 1.5 Kbytes.
Bit 9	Reserved
Bit 10	Write-Violation
	In total parameter cells in the RAM were overridden externally, the SPC 4-2 changes to the offline state.
Bit 11	Reserved
Bit 12	Reserved
Bit 13	FIFO overflow
	FIFO overflow when receiving; reception not stopped (this should never occur since the SPC 4-2 never accesses the internal RAM with lock activated in the FF mode).
Bit 14	Reserved
Bit 15	IND
	Frame received error-free

Table 7-23 : Interrupt Register in FF Mode

7.10 Clock Synchronization

Description

Clock synchronization is triggered by a global control frame (SD2 to SAP58). The SPC 4-2 handles all global control frames like the SPC 4-1. In addition, however, when the GCT is error-free, it compares the station address contained in the frame with a station address set in the internal RAM (test for valid constant-time scan master). It also compares the group byte in the frame with a group address that is also set in the internal RAM. If both of these match, a counter is clocked. If the counter reaches the end value set in the new "Counter end value" register, the counter is cleared and the MEM-OVERFLOW interrupt is activated. The SPC 4-2 has a new register for the counter end value (address 0x31F, write only)

Bit 5 of the status register (Early-Ready) is used to distinguish between an actual memory overflow and the clock synchronization event: the interrupt is a clock synchronization only when this bit is set to 1. The previous function of the Early-Ready bit is therefore no longer available in the SPC 4-2 mode. The interrupt register bit TAKT_SYNC (available only internally) is switched to the SPC 4-2 output XINTCI without masking and remains active (zero-active) until the software clears the interrupt. XINTCI is therefore a new, non-maskable interrupt output.

To activate clock synchronization, the "Enable-SPC 4-2" bit must be set in mode register 4, only then is access to the three new registers possible. The "Enable-Takt-Sync" bit must also be set in mode register 4. This activates the new microprogram section and connects the XINTCI output with the interrupt.

The station address of the valid constant scan time master is stored in the RAM parameter block at address 0x006. The group-select byte is stored in the ram parameter block at address 0x007. As a result, the monitoring range of the write violation interrupt in the SPC 4-2-mode changes by two byte addresses (previously RAM address 6 to 23_{dec}, now 8 to $23_{dec)}$.

The clock synchronization output XINTCI of the SPC 4-2 is active when a clock synchronization event occurs at the earliest $_{delay\text{-}min}$ and at the latest $T_{delay\text{-}max}$ after the end of the frame (end of the end delimiter in PA or end of the stop bit in DP). The difference between $T_{delay\text{-}max}$ and $T_{delay\text{-}min}$ is known as jitter. In the PA mode, both delay times depend on the GCT frame length used, LE = 6 and LE = 7 are possible.

T_{bit} is the period of the baud rate used.

T_{spc4} is the period of the SPC 4-2 input clock.

This results in the following:

For DP:

$T_{delay-min}$: 3.25 T_{bit}
Jitter: 0.5 T_{bit}

The use of the digital filter in DP increases the jitter by T_{spc4}.

For PA (LE = 6):

$T_{delay-min}$: 17.875 T_{bit}
Jitter: 2.0 T_{bit}

For PA (LE = 7):

$T_{delay-min}$: 11.875 T_{bit}
Jitter: 1.0 T_{bit}

The use of pulse modulation increases the jitter by T_{spc4}.

As a comparison, the values of the DPC31 are shown below (see specification DPC31 version 1.0):

T_{delay}: 250 ns
Jitter: 0.25 T_{bit} + T_{48}

7.11 SPC 4-2-Timers

7.11.1 Delay Timer

Description

The delay timer on the SPC 4-2 is implemented as a 24-bit timer. To remain compatible with SPC 4, the delay timer is limited to 16 bits in the PA mode (XPB/PA=1).. It is automatically reset and started when a "first-time frame" is received. The counter is incremented until it is read. At each overrun, an interrupt (Del-Tim-Overrun) is generated and incremented.

The counter reading must be reset after it is read out so that no further delay timer overrun interrupt is generated and so that the system management can recognize when a second SM-Time frame arrives (for example, if the first SM-Time frame was lost due to a bus problem), for further details refer to system management (SM-Time). System management must be capable of handling possible error situations such as two consecutive second SM-Time frames from different time masters.

The FAKT_DEL_CLK divider has a range from 64 to 1536.

$$FAKT\_DEL\_CLK = \frac{Quarz}{DEL\_CLK} - 1$$

Quartz	FAKT_DEL_CLK	DEL_CLK	Resolution=1/DEL_CLK
48 MHz	1535	31.25 kHz	32 µs
20 MHz	639	31.25 kHz	32 µs
2 MHz	63	31.25 kHz	32 µs

Table 7-24 : Formula for Calculating FAKT_DEL_CLK

Note

According to PROFIBUS-PA a resolution of 32 µs should be selected, the divider FAKT_DEL_CLK must be set depending on the required quartz frequency.
When selecting the quartz frequency, the table for the baud rate generator must be taken into account.

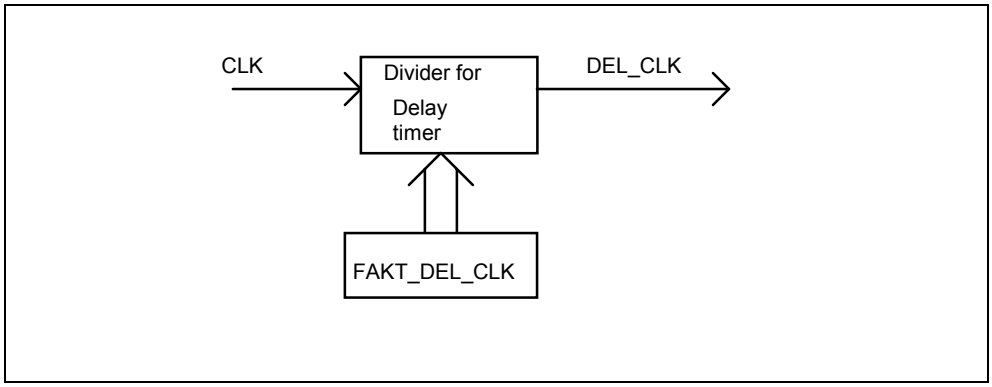

Figure 7-25 Delay Timer Function (1)

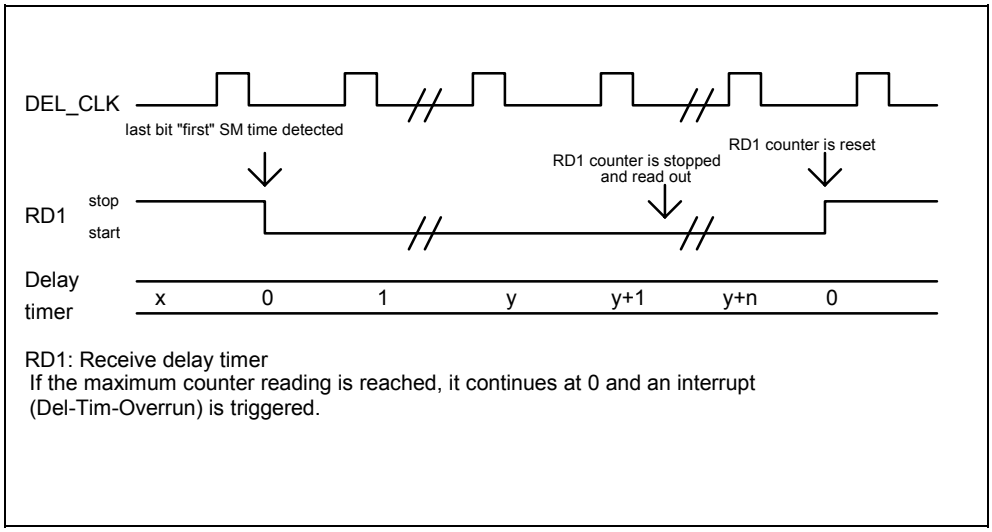

Figure 7-26 Delay Timer Function (2)

7.11.2 Idle Timer

Description

This timer controls the idle phase directly on the internal bus line RxD/RxA (logical '1'). Depending on the frame type, the following times must be monitored:

TSYN

TSYN:The synchronization time TSYN is the minimum time during which each node must detect the idle state on the transmission medium before it is allowed to accept the start of a call or token frame.

In the asynchronous mode, the Syn-Time is 33 bits.

In the synchronous mode, the Syn-Time can be selected. The valid value is located in the SYN-Time register and is between 4 and 32 bits. [3]

TRDY

The TRDY ready time is the time that must elapse as an idle phase on the transmission medium at the responder after receiving the call frame before it is permitted to send its response/acknowledgment frame. TRDY is selected in the TRDY register.[4]

7.11.3 Syni-Timer

Description

This timer is used to monitor the transmission medium to determine whether or not receiver synchronization takes place within the TSYNI time. The timer is reset at the first activity on the line after the idle time has elapsed and is incremented with BRCLK . The timer is stopped when the idle timer lapses. The idle timer therefore controls the syni timer directly. If the idle timer is running, the syni timer is enabled and vice-versa . If there is a problem on the transmission medium, for example permanent logical '0' or a permanent alternation between '0'/'1' in the asynchronous mode or permanent activity in the synchronous mode, the idle timer does not stop (no synchronization is then possible): The syni timer them increments to the value TSYNI = 11385 bits or 8672 bits in synchronous transmission and then stops. The SPC 4-2 them generates the Error-Interrupt Syni-Error.

After a reset, the syni timer (14 bits) is disabled. It is started specifically by "START-SPC 4-2 = 1" (mode register 1) following initialization.

3 The PNO Guideline PROFIBUS PA Version 1.0 defines T_{SYN}=28...112 bits. This definition, however, includes the preamble and the delimiters. If, however, the IDLE timer is reset with the XRxA signal, these parts must not be included.
4 The TRDY time defined here corresponds to the "min T_{SDR}" time as defined in DIN 19245 or for PROFIBUS PA. In the synchronous mode, TRDY=T_{IFG} (interframe gap time).

7.11.4 Slot Timer

Description

This timer generates the count intervals for the time-out timer.

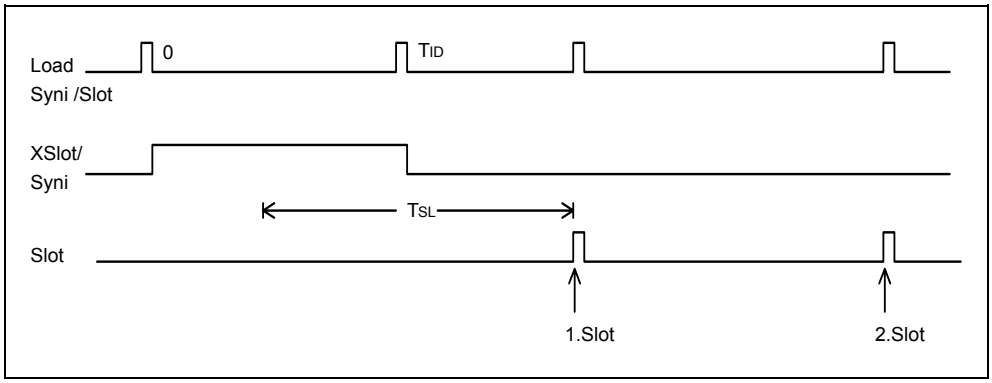

Figure 7-27 Controlling the Slot Timer

The slot timer is a cyclic timer that increments with BRCLK. It is loaded with the idle time at the start. It runs only in the phases when the syni timer is stopped. For this reason, a common syni/slot timer (14 bits) is used.

In all MAC states (apart from offline), the slot timer elapsing causes the timeout timer to increment and the slot timer is loaded with the value '0' and restarted. With the next BRCLK, it has the value '1'.

Following initialization, the syni/slot timer is started as the syni timer ("START-SPC 4-2 = 1").

7.11.5 Timeout Timer

Description

The Timeout timer is used to monitor bus activity on the serial interface. $T_{TIMEOUT}$ is a multiple of the slot time. The SPC 4-2 calculates this time according to the formulae "$T_{TIMEOUT} = (130 * 2 + 6) * T_{SLOT}$" for passive nodes before it leaves the offline state.

The timeout timer (9-bit) is a one-shot-timer that increments at the slot interval rate (TO_{CLK}). The controller takes the XSlot/Syni status bit. If the Syni-timer is running (XSlot/Syni = 1), the timeout timer is locked. With the change from Syni to Slot (XSlot/Syni = 0), the timeout timer is cleared, enabled, and incremented at each TOCLK (slot interval). If there is activity again on the serial bus before the timeout timer elapses (XSlot/Syni = 1), the controller stops the timer again.

When the timer elapses, the timeout status flag is set and the timer is stopped.

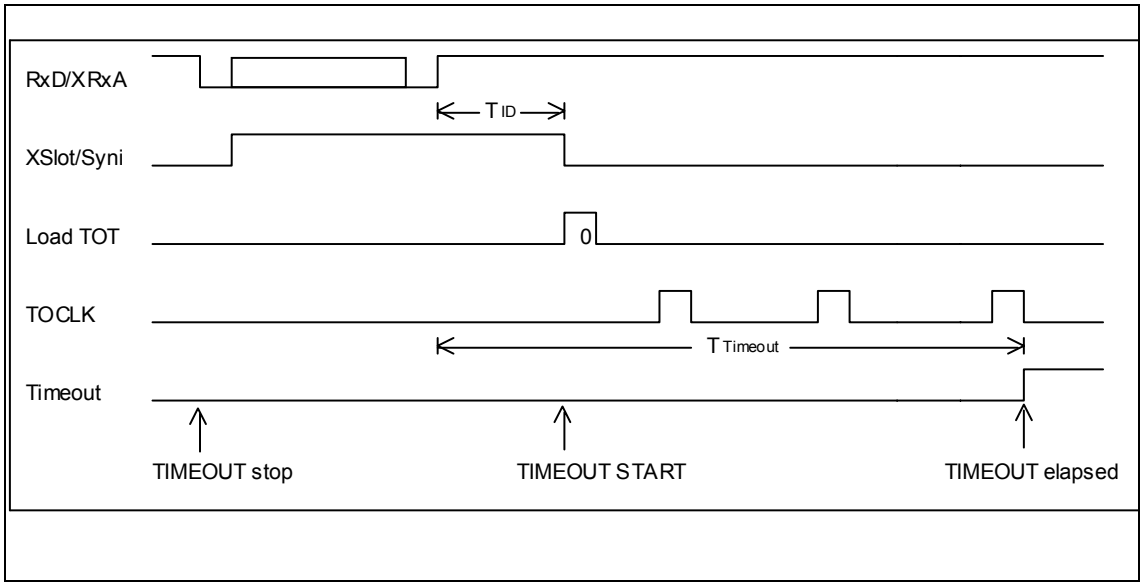

Figure 7-28 Control of the Timeout Timer

7.11.6 New Timers in the FF Mode

Description

The SPC 4-2 contains 4 new 16-bit timers. These can be used only in the FF mode since they use interrupt bits that are only free in the FF mode. They all run at the baud rate speed.

In the timer type register, the user can set the timers either as "one-shot" or as "cyclic" timers.

The timers are started, stopped, and resumed using the new timer control register.

A timer can only be started when its start value has been entered in the timer register. When it starts, each timer loads the start value from its start value register and counts down until it reaches the value 0. It then triggers an interrupt. The "cyclic" timer then goes back to its start value immediately and starts counting again, while the "one-shot" timer remains at 0.

To start a "one-shot" timer again after it has elapsed, the user simply needs to write a start command to the timer control register again. If you want to retrigger a "one-shot" timer that has not yet elapsed, you must first stop the timer and then start it again. This also applies when it is used as a "cyclic" timer. The user must first stop the counter by writing "11" to the relevant bits of the control register before the timer can start or continue counting with a start command (by writing "01" or "10" to the relevant bits).

A resume counting command to a previously stopped counter starts the counter from the start value again if the counter had reached 0 when it stopped.

To ensure that the higher byte always matches the lower byte when reading out the timer values via the 8-bit data bus, the user must **always** read the lower byte first and **then** the higher byte (while the lower byte is being read, the higher byte is copied to register and it is then read from this register). Word access to this register is therefore not permitted.

Note

Between all operations with timers (for example, stopping and restarting), always wait one clock period of the timer clock pulse rate.

Timer-Type Register (address 0x31D; write only):

Bit 0		
	0	Timer0 is a cyclic timer (status following reset).
	1	Timer0 is a "one-shot" timer
Bit 1		
	0	Timer1 is a cyclic timer (status following reset).
	1	Timer1 is a "one-shot" timer
Bit 2		
	0	Timer2 is a cyclic timer (status following reset).
	1	Timer2 is a "one-shot" timer
Bit 3		
	0	Timer3 is a cyclic timer (status following reset).
	1	Timer3 is a "one-shot" timer

Timer-Control Register (address 0x31E; write only):

Bit (1:0)		
	00	Status of Timer0 remains unchanged.
	01	Timer0 is restarted at the start value.
	10	Timer0 resumes count (only effective if timer was previously stopped).
	11	Timer0 is stopped.
Bit (3:2)		
	00	Status of Timer1 remains unchanged.
	01	Timer1 is restarted at the start value.
	10	Timer1 resumes count (only effective if timer was previously stopped).
	11	Timer1 is stopped.
Bit (5:4)		
	00	Status of Timer2 remains unchanged.
	01	Timer2 is restarted at the start value.
	10	Timer2 resumes count (only effective if timer was previously stopped).
	11	Timer2 is stopped.
Bit (7:6)		
	00	Status of Timer3 remains unchanged.
	01	Timer3 is restarted at the start value.
	10	Timer3 resumes count (only effective if timer was previously stopped).
	11	Timer3 is stopped.

Address of the Counter Register	**Bit Position**								**Meaning**
	7	6	5	4	3	2	1	0	
$0x320_H$	T0_15	T0_14	T0_13	T0_12	T0_11	T0_10	T0_9	T0_8	Timer0-Reg Bit 15-8
$0x321_H$	T0_7	T0_6	T0_5	T0_4	T0_3	T0_2	T0_1	T0_0	Timer0-Reg Bit 7-0
$0x322_H$	T1_15	T1_14	T1_13	T1_12	T1_11	T1_10	T1_9	T1_8	Timer1-Reg Bit 15-8
$0x323_H$	T1_7	T1_6	T1_5	T1_4	T1_3	T1_2	T1_1	T1_0	Timer1-Reg Bit 7-0
$0x324_H$	T2_15	T2_14	T2_13	T2_12	T2_11	T2_10	T2_9	T2_8	Timer2-Reg Bit 15-8
$0x325_H$	T2_7	T2_6	T2_5	T2_4	T2_3	T2_2	T2_1	T2_0	Timer2-Reg Bit 7-0
$0x326_H$	T3_15	T3_14	T3_13	T3_12	T3_11	T3_10	T3_9	T3_8	Timer3-Reg Bit 15-8
$0x327_H$	T3_7	T3_6	T3_5	T3_4	T3_3	T3_2	T3_1	T3_0	Timer3-Reg Bit 7-0

Asynchronous Interface 8

8.1 Baud Rate Generator

Description

The baud rate generator (BRG) provides all the clock rates required on the SPC 4-2 for transmitting data in the asynchronous UART format at the following data rates:

9.60 Kbps
19.20 Kbps
93.75 Kbps
187.50 Kbps
500.00 Kbps
1.50 Mbps
3.00 Mbps
6.00 Mbps
12.00 Mbps

8.2 Transmitter

Description

The transmitter converts the parallel data structure into a serial data stream with a start bit, 8 data bits, an even parity bit and a stop bit. The **least-significant data bit is sent first.** Request-to-Send (RTS) is generated before the first character. The XCTS input is available for connecting a modem. Following RTS active, the transmitter must hold back the first frame character until the modem activates XCTS.

8.3 Transmitter

Description

The receiver converts the serial data stream into a parallel data structure. It scans the serial data stream at 4 x the transmission rate (at 12 Mbps) or at 16 x the transmission rate. Synchronization of the receiver always begins at the negative-going edge of the start bit. The start bit and the other bits are scanned three times at the bit mid point at data rates ≤ 1.5 Mbps. The value for the start bit must be logical '0' and for the stop bit logical '1'. With the data bits and the parity bit, the receiver makes a two out of the three majority decision. If the receiver detects three "zeros" at the bit mid point when scanning the start bit, it aborts synchronization. The stop bit with 3 x logical '1' completes correct synchronization. If any scanned value is not "1", this is interpreted as ERR-UART. The receiver also checks the parity bit and also signals ERR-UART if it does not match.

8.4 Serial Bus Interface PROFIBUS Interface (Asynchronous)

8.4.1 Interface Signals

Data transmission is in the RS-485 mode (RS-485 physical bus characteristics).

The SPC 4-2 must be connected to the electrically isolated interface drivers with the following signals:

Signal Names	I/O	Type	Note
TxD	L	non Tristate	Transmit data
RxD	I		Received data
RTS	O	non Tristate	Transmit driver enable
XCTS	I		Transmitter enable

Table 8-1: Interface Signals

Pinout

If the interface is to be designed as a standard-compliant PROFIBUS interface with a 9-pin sub-D female connector, keep to the following pin assignment:
Pin 1 - free
Pin 2 - free
Pin 3 - B line
Pin 4 - Request to send (RTS)
Pin 5 - Data ground (M5)
Pin 6 – Power supply plus 5V (floating P5, current depending on connected device, min. 10 mA)
Pin 7 - free
Pin 8 - A line
Pin 9 - free

The cable shield must be connected to the housing.

The required current at pin 6 (P5) depends on the device to be connected:

- Terminating resistor in bus connector / bus terminal (complying with DIN19245): approx. 10 mA
- ET200 Handheld: approx. 50 mA
- Optical bus terminal SF/PF: approx. 90 mA

The use of the free pins is optional but should comply with DIN E 19245 Part 3.

Notice:

- The names **A** and **B** of the lines of the connector comply with the names in the RS-485 standard and not with those of the pin names of the driver ICs.
- The wire length from the driver to the connector must be kept as short as possible.

8.4.2 RS-485 Timing

Description

Before transmitting, the SPC 4-2 sets the RTS signal to "1" and then loads the transmit buffer of the UART with the first character. The UART delays the first character of the frame until the XCTS signal is active. During transmission, CTS is no longer queried. On completion of transmission (buffer empty stop bit is sent), RTS is reset. The XCTS must be set to log.<0> during operation.

Switching times:

No	Symbol	Parameters	min.	Unit
1	TsRTS (TXD)	RTS ↑ to TXD (setup time)	1.5	TBit*
2	ThRTS (TXD)	RTS ↓ to TXD (hold time)	1	TBit*

*: 1 TBit = 104μs at 9.6 kbauds, 1 TBit = 83ns at 12 Mbauds

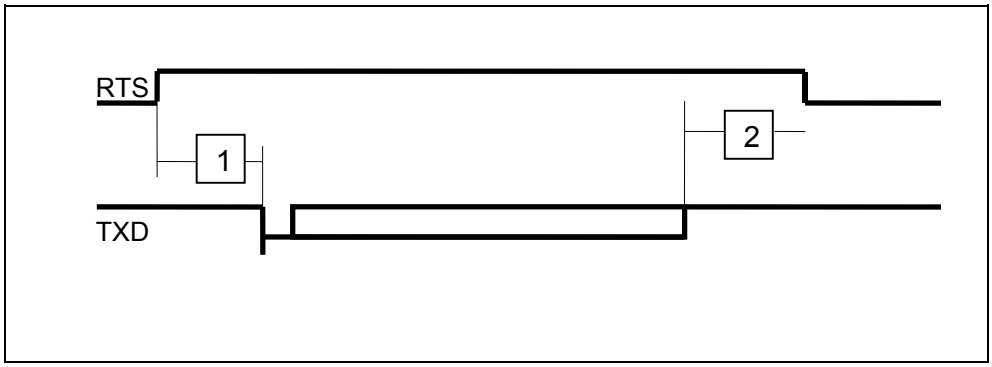

Figure 8-2 RS-485 Timing

8.4.3 Suggested Wiring for RS-485

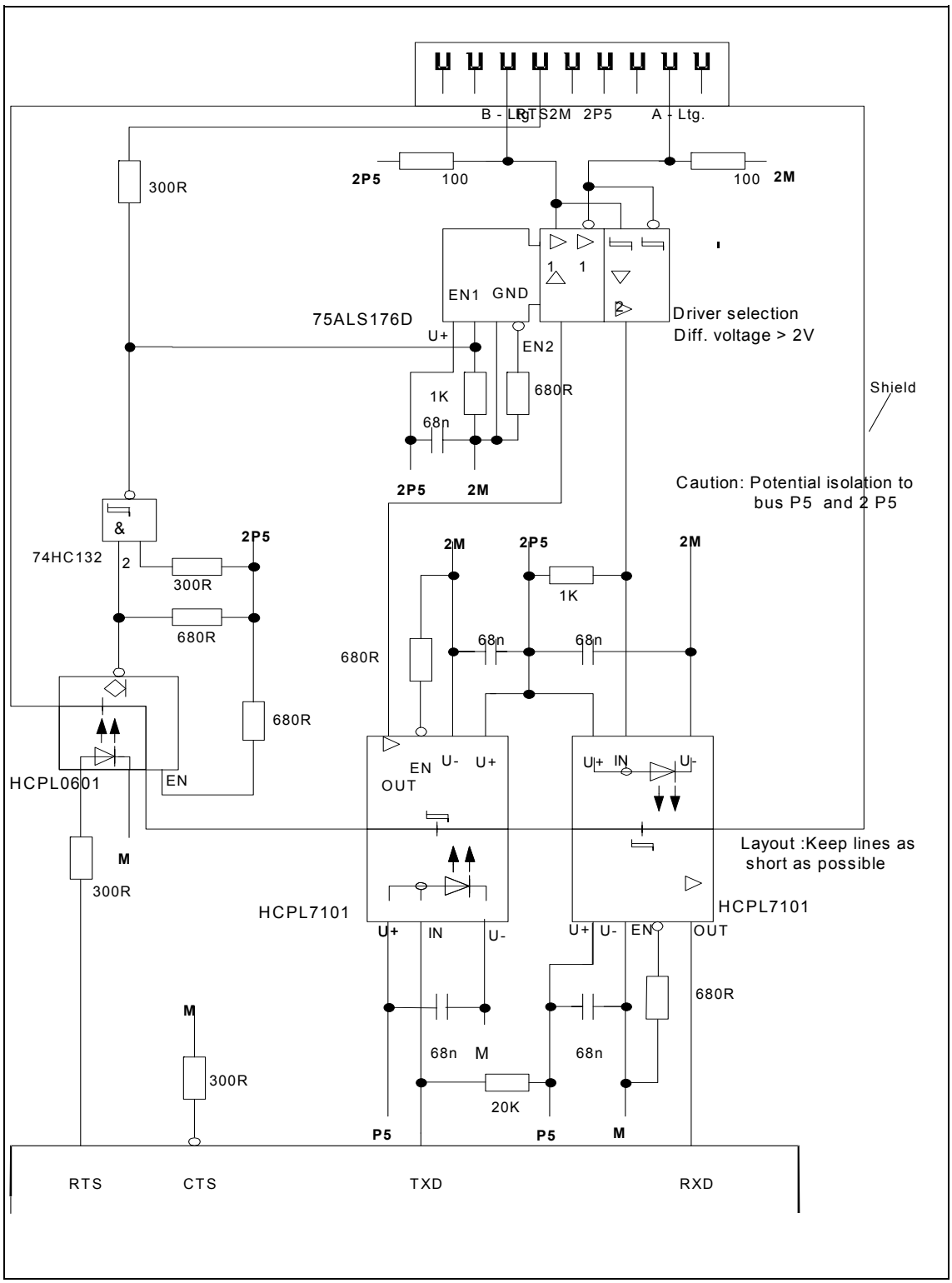

Figure 8-3 Circuit Diagram

Synchronous Interface 9

9.1 Overview

Description

The synchronous interface allows data transmission complying with IEC 61158-2 (voltage mode, 31.25 Kbps). It includes services of the interfaces defined in this standard between the data link layer and physical layer **(FDL-Ph Layer Interface)**, the Ph DIS sublayer**(DCE Independent Sublayer)** and Ph MDS **(Medium-Dependent Sublayer)** for wire media and the corresponding **MDS-MAU Interface**. The **Station Management-Physical Layer Interface** (parts of the service primitives defined optionally in the IEC 61158-2 standard) is also implemented. What is not implemented is the so-called "Medium Access Unit" (MAU) that includes the transmit pulse shaper, the line driver, the receive amplifier, the receive filter, and the line attachment (if necessary with remote powering). The MAU ASIC SIM1 simplifies the structure of this synchronous interface significantly (refer to the appendix or the separate description).

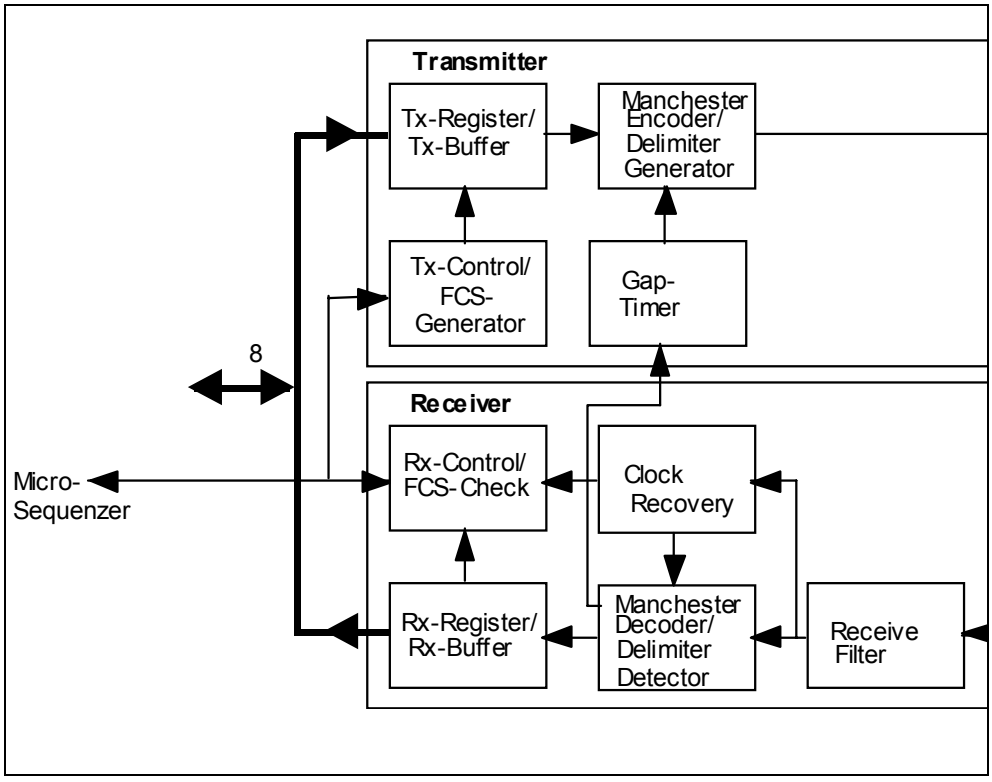

Figure 9-1 Block Diagram of the Synchronous Interface

9.2 Baud Rate Generator

Description

The baud rate generator can generate the data rate 31.25 Kbps.

9.3 Transmitter

Description

The transmitter converts the parallel data structure to a serial data stream. Synchronous transmission complying with IEC 1158-2 uses Manchester coding and start and end delimiters. Each frame is preceded by a preamble. The length of the preamble is stored in the PREAMBLE register. **The most significant data bit (in contrast to the asynchronous interface) is set first** [5]**.** The transmitter generates a 16-bit CRC field and appends it to the data field.

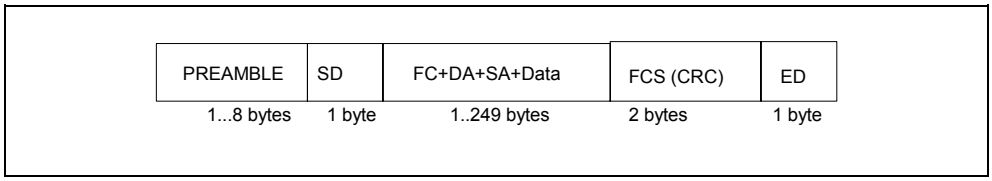

Figure 9-2 Frame Structure of the Serial Interface

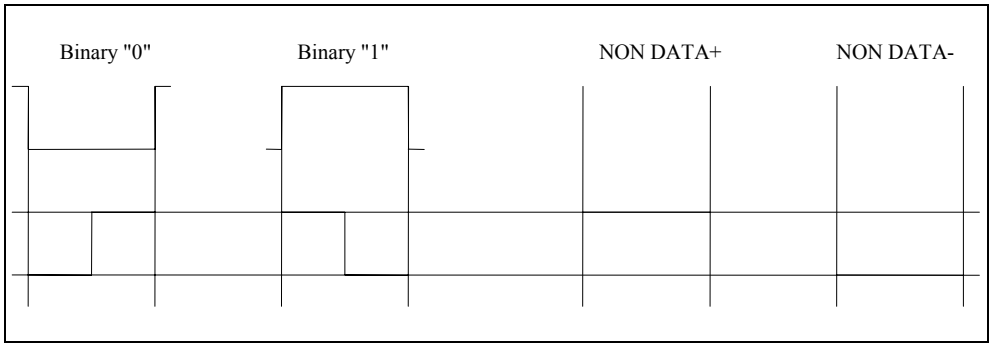

Figure 9-3 Bit Coding of the Synchronous Interface

[5] According to IEC 61158-2, Chapter 7.

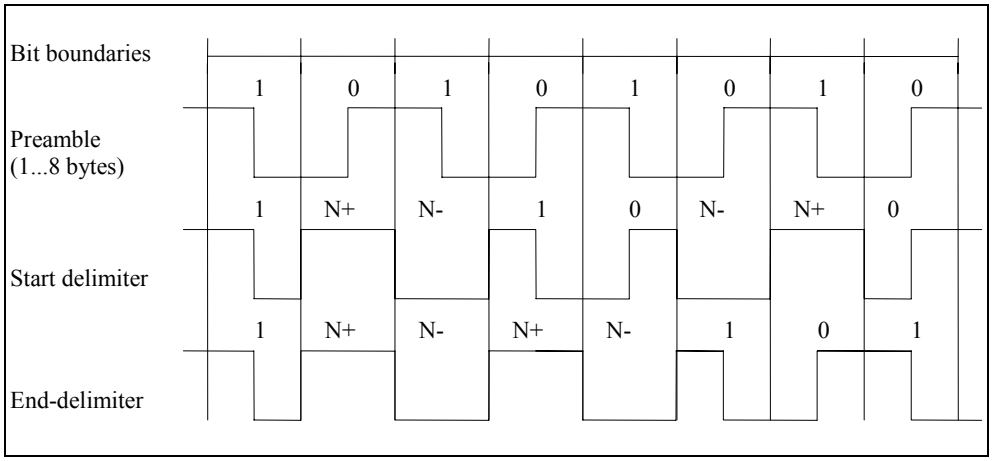

Figure 9-4 Bit Coding of the Synchronous Interface

The transmitter provides various output signals:

- RTS (request to send)
- TxS (transmit signal)
- ADD (add signal).

With the combination of TxS and ADD it is extremely easy to implement an adder circuit to control a current control unit as is used in the interface of an intrinsically safe bus node. The combination RxS/TxS is an advantage when controlling a transformer.

The RTS and ADD signals are applied to a common output (RTS/ADD). The switchover between two modes can be set with parameters in mode register 0.

To guarantee the minimum gap between two frames, the transmitter is locked after the end of the frame for a time known as a the minimum interframe gap time. The gap timer is loaded with the current value of the interframe gap time from the SYN-time register.

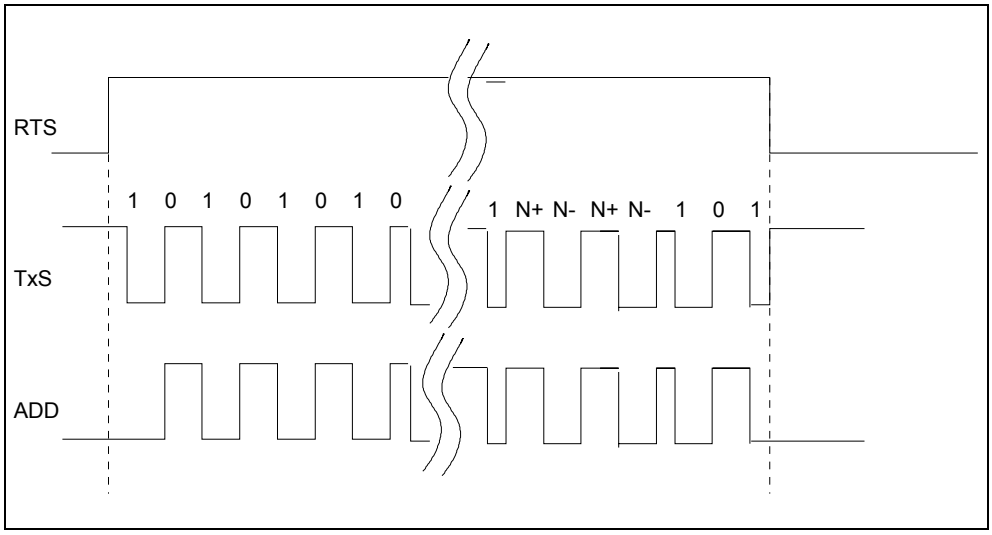

Figure 9-5 Output Signals of the Synchronous Transmitter

9.4 Receiver

Description

The receive filter is responsible for conditioning the received signal RxS for clock recovery and clock decoding.

The Manchester decoder obtains the data from the filtered received signal.

The clock recovery function obtains the CLK1 clock from the filtered received signal.

The data decoder scans the filtered received signal at the recovered received clock rate RxC (positive edge) and passes on the scanned value weighted with the polarity information transferred by the decoder state machine (POL=1 or POL=0) as the received signal RxD.

9.5 Pulse Modulation in the SPC 4-2

The SPC 4-2 has circuits for a direct connection SIM1-optocoupler-SPC 4-2 (PROFIBUS PA attachment) using the current-saving interface of the SIM 1. A separate adapter circuit is no longer necessary.

The circuit is designed for a single application:

PROFIBUS-PA

Operating frequency on SPC 4-2: 2 MHz

Baud rate: 31.25 kbauds

Description

The frames received from SIM1 are not passed on to the SPC 4-2 in their original form. To save current, the SIM converts the frame to a series of short pulses. It therefore appears at the SPC 4-2 in the following form:

Each rising edge in the frame produces a high pulse with a width of 5µs, each falling edge a high pulse with a width of 2µs: between pulses, the signal is level 0.

The original frame is recovered in the receive unit.

When a frame is sent by the SPC 4-2 , this pulse train is generated from the frame to be sent. The only difference is the inverted polarity: To activate the optocoupler, low pulses must be generated instead of high pulses.

Activation:

To start the pulse modulation the user must set the pulse modulation bit in mode register 3 (address 31BH).

Pulse modulation (bit 0):	0:	pulse modulation is deactivated (status following reset).
	1:	Pulse modulation is enabled.

9.6 Pulse Demodulation

Description

The permitted pulse widths of the pulse interface are specified in the SIM 1 specification. Here, 2 µs ± 0.5 µs is specified for a short pulse and 5 µs –0.5 µs/+2 µs for a long pulse.

For demodulation of the pulses, the SIM1 specification specifies a timing element with a time of 2.9 µs to 3.2 µs (t3, see SIM1 specification). This timing element was, however, implemented digitally so that the SIM1 recognizes pulses shorter than 3.0 µs and longer than 3.5 µs accurately. Pulse widths between these limits are detected at random as "short" or "long" pulses.

On the SPC 4-2, the window in which the pulse width is unreliably detected can be shifted:

Uncertainty window SPC 4-2:

2.5 µs to 3.0 µs scan mode 00
3.0 µs to 3.5 µs scan mode 01 (following reset)
3.5 µs to 4.0 µs scan mode 10
4.0 µs to 4.5 µs scan mode 11

Being able to shift the window simplifies the selection of the optocouplers between SIM 1 and SPC 4-2. The uncertainty window of the SPC 4-2 can be set in the new mode register 4 (see Section 7.1.11). Following a reset, it is set between 3.0 µs and 3.5 µs.

9.7 Fast Synchronizer in the Manchester Receiver

Description

Fast synchronization means finding the bit mid point in the preamble of a Manchester frame (PROFIBUS PA). The SPC4 sets this point on the fourth frame edge in the preamble. The SPC 4-2 attempts to identify this point more accurately by determining the duration of the last high and low phase before the fourth edge. From the average of the these two numbers, it calculates a correction value that is taken into account when identifying the midpoint of the bit. With this modification, the SPC 4-2 can handle more system distortion (all rising or falling edges are delayed by the same amount) than the SPC4..

To activate this improved synchronization mode, the user must set the "Quick_Sync_New" bit in mode register 3 (address 31BH):

Quick_Sync_New (bit 2):	0:	improved mode inactive (status following reset)
	1:	improved mode active

Clock Pulses

10

Clock pulses at QCLK-IN

Operating voltage	Transmission mode	Clock max. = 1/T
5 V	asynchronous	48 MHz
5 V	synchronous	40 MHz
3.3 V	asynchronous	20 MHz
3.3 V	synchronous	16 MHz

Clock timing:

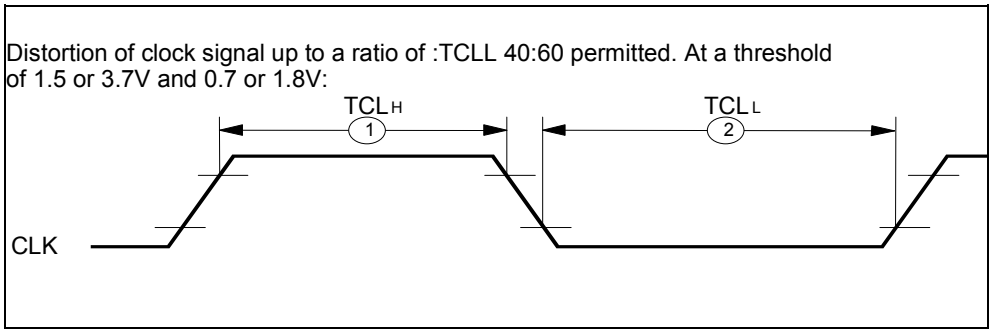

Figure 10-1 Clock Timing

Quartz connection:

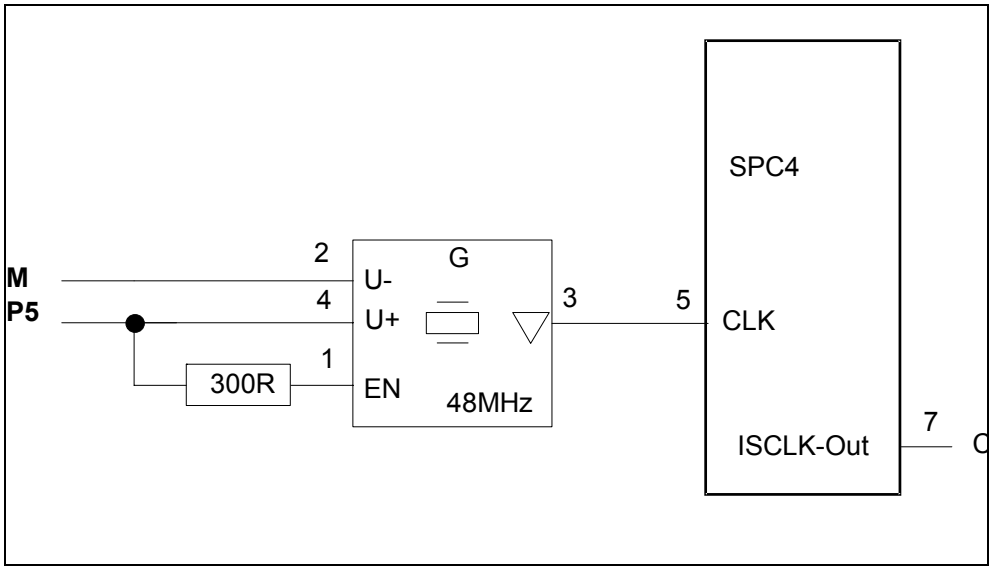

Figure 10-2 Quartz Connection

From a connected quartz, the **clock generator** generates the internal CLK, from which all the clock signals required on the SPC 4-2 are generated. The base clock rate is provided to other components (for example the processor) via a selectable divider (Pin 3 "0"=:4, "1"=:2 divided clock rate).

With the HC11 Motorola family, the E-clock must only be ¼ of the input clock rate of the SPC 4-2 (Osc.)

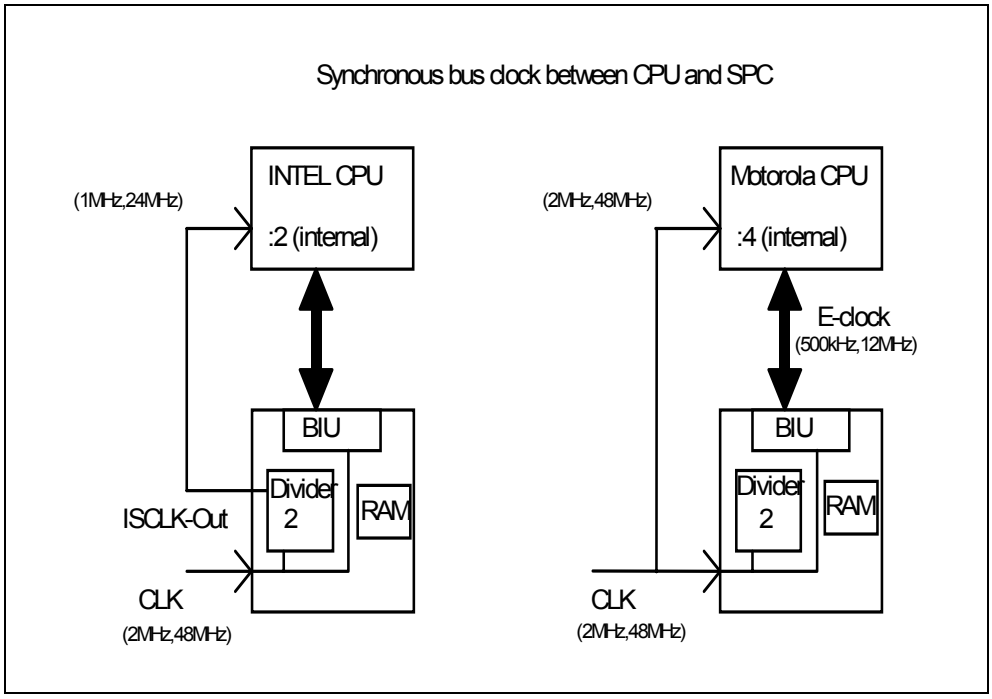

Figure 10-3 Overview of the Connection Scheme for INTEL and Motorola CPUs with Synchronous Bus Timing

Processor Interface 11

11.1 Universal Processor Interface

Description

The SPC 4-2 has a parallel 8-bit interface with a 10-bit address bus. It supports all 8-bit microcontrollers whose CPU is based on the 80C51/52 (80C32) line from INTEL, the MOTOROLA HC11 family, and the 8/16-bit microcontroller of the 80C166 family from SIEMENS, X86-compatable processors from Intel and the HC16 and HC916 family from MOTOROLA.

A clock divider is also integrated that provides the internal working clock rate divided by 2 or 4 for external use and therefore allows low-cost systems to be implemented.

Since the data formats of Intel and Motorola processors are not compatible, the SPC 4-2 automatically performs **'byte swapping'** when access is in words **(only when writing or reading a 16-bit register in the parameter area; all other parameters must be accessed byte-oriented)**. This allows a Motorola processor to read the 16-bit value correctly. As usual, reading or writing requires two accesses (8-bit data bus). With the two configuration pins TYPE and MODE, the interface can support the different microcontroller types and their bus timing as required (read and write cycles). . The TYPE pin decides the data format for the microcontroller family and the MODE pin decides synchronous (rigid) or asynchronous bus timing. The "divider" pin can also be used to set a clock rate divided by 2 or 4 at the ISCLK-Out pin.

TYPE and MODE

TYPE , MODE	The SPC 4-2 interface supports the following microcontroller
1 1 (synchronous Motorola)	MOTOROLA microcontroller with the following characteristics: • Synchronous (rigid) bus; timing without evaluation of the READY signal • 8-bit non-multiplexed bus: DB(7-0), AB(9-0) The following can be connected: • HC11 types: K, N, M and F1 • HC16 and HC916 types with programmable ECLK timing All other HC11 types with a multiplex bus must select the addresses A(7-0) externally from the data D(7-0). The address decoder is deactivated on the SPC 4-2; CS signal is supplied to the SPC 4-2: • On microcontrollers with chip-select logic: K, F1, HC16, HC916 are the chip-select signals that can be programmed in terms of address range, priority, polarity and the window width in the write or read cycle. • On microcontrollers without chip-select logic; N, M and others require an external chip-select logic. This means additional hardware investment and fixed assignments. Condition: SPC 4-2 clock (QCLK-IN) must be at least four times higher than the required bus clock rate (E-clock rate).
1 0 (asynchronous Motorola)	MOTOROLA microcontroller with the following characteristics: • Asynchronous bus; timing with evaluation of the READY signal • 8-bit non-multiplexed bus: DB(7-0); AB(9-0) The following can be connected: • HC16 and HC916 types Address decoder on the SPC 4-2 is deactivated; CS signal is supplied to the SPC 4-2: The chip-select signal exists on all microcontrollers and can be programmed.
0 1 (synchronous INTEL)	INTEL, CPU Basis 80C51/2 (80C32), microcontrollers from various vendors • Synchronous (rigid) bus; timing without evaluation of the READY signal • 8-bit multiplexed bus ADB(7-0), The following can be connected: • Microcontroller families, e.g. INTEL, SIEMENS, PHILIPS ... Address decoder on the SPC 4-2 is activated; CS signal is supplied internally: • The lower address bits A(7-0) are stored in an internal address latch with the ALE signal. On the SPC 4-2 , the internal CS decoder is activated and generates its own CS signal from the address A(9- 0). • The integrated address decoder is hardwired so that the SPC 4-2 must always be addressed at the fixed address at A(7...0)=0000 00xxb , and the SPC 4-2 selects the corresponding address window from the signals A(1,0) . • In this mode, the CS pin (XCS) must be connected to VDD (high potential) Wiring: Connection diagrams are stipulated by the specification. • ADB(7-0) to SPC 4-2 pin DB(7-0), AB(15-8) to SPC 4-2 pin • AB(7-0) and SPC 4-2 pin AB (9,8) connected to VSS. • SPC 4-2 clock (QCLK-IN) must be at least four times higher than the required bus clock rate.

TYPE , MODE	The SPC 4-2 interface supports the following microcontroller
0 0 (asynchronous INTEL)	INTEL and SIEMENS 16-/8-bit microcontroller families • Asynchronous bus; timing with evaluation of the XREADY signal • 8-bit non-multiplexed bus: DB(7-0); AB(9-0) The following can be connected: • Microcontroller families, e.g. SIEMENS, 80C16x and INTEL X86 Address decoder on the SPC 4-2 is deactivated; CS signal is supplied to the SPC 4-2 • External address decoding is always required External chip-select logic if this does not exist on the microcontroller **Note:** Bit X86 in mode register 2 must be set for this mode.

11.2 Bus Interface Unit (BIU)

Description

The bus interface unit provides the interface to the microcontroller. It allows the connected microcontroller access to the internal 3-Kbyte dual port RAM. Depending on the connected microcontroller types, the BIU generates the request signals for the dual-port RAM controller from the control signals (ALE with internally generated CS signal or E-clock rate with an externally applied CS signal.

11.3 Dual-Port RAM Controller

11.3.1 Function

The internal maximal 3-Kbyte RAM of the SPC 4-2 is a single-port-RAM. Control by an integrated dual-port RAM controller (DPC) , however, allows almost simultaneous access by both ports (bus interface and microsequencer interface MS). Since access via the external interface takes significantly longer than the MS access, they can be interleaved so that the externally connected processor does not recognize any delay.

An external bus request is generated by the BIU and passed on to the DP-RAM controller. A request is formed differently depending on the mode:

In the configuration mode (1,1) for Motorola microcontrollers, the rising edge of the e-clock pulse is evaluated as a request if the CS signal is present at the same time.

In the Motorola asynchronous configuration mode (1,0) the falling edge of AS is evaluated as a request if chip-select is also activated.

In the Intel 80C32 configuration mode (0,1), the falling edge of the read-write signal to be synchronized is evaluated as a request when the internal CS decoder generates a CS signal at the same time.

In the Intel X86 configuration mode (0,0), the falling edge of the read-write signal to be synchronized is differentiated and in this case the CS signal is evaluated.

In the 80C165 configuration mode (0,0), the falling edge of ALE triggers access and the chip-select signal is evaluated.

Notice:

The local microprocessor interface is decoupled from the actual DPRAM by a buffer and by the DPRAM controller. When the DPRAM is written to, the information is only physically present when at least four active 0-1 edges of the SPC4-2 clock pulse have occurred since the active write edge of the local interface (regardless of the local microprocessor interface). This means that back-to-back accesses to the DPRAM cannot be faster than is required for two successive write edges with at least four clock periods between them. The same applies following write when data is to be read from the same cell immediately.

11.3.2 Access to the SPC 4-2 with LOCK Activated

Description

In the dual-port RAM certain areas are modified both by the FLC and by the MS; these are cells in the SAP list. To avoid data conflicts between write and read-modify-write access, the SPC 4-2 has a lock mechanism (see also the hardware description, section 5.1.2). If the FLC wants to access this area, it must first check whether the memory is 'locked' by the MS. For this purpose, there is a symbolic memory cell 'Mem-Lock' (in other words, a reserved address), in the address area of the parameter latches. The value of this cell is switched to bit(0) of the data bus when it is read.

If the value = 'logical 0', the memory bus is not locked by the microsequencer and the FLC can access the RAM in the next cycle. As soon as the cell is read, an internal lock flag is set. With this flag, the dual-port RAM controller recognizes that there has been access via the interface with LOCK activated. If the MS also wants to access with LOCK activated at this point in time, the dual-port RAM controller (DPC) stops the MS. As a result, if the FLC reads 'logical 0' when accessing the mem-lock cell, the next accesses are made with the lock activated until the flag is reset.

If the mem-lock cell returns a 'logical 1', the MS is currently accessing the RAM with LOCK activated. In this case, the FLC must poll the mem-lock cell until a 'logical 0' is returned. Generally, the bit will be reset the second time it is read, since MS access is considerably faster than read access via the external interface.

Notice:

In particular in cases is which the local microprocessor has a much faster clock rate than the SPC 4-2, it cannot be assumed that local microsequencer access will be faster than access by the microprocessor. Polling the mem-lock cell is absolutely necessary here.

The state of the MEM-LOCK bit is entered in the status register. After access with lock activated, the bit must be reset. This achieved by a byte cycle to the mem-lock cell, with don't care data.

Note

The duration of the lock must be less than the maximum selected T_{ID1} or T_{SLOT} of the master station. If this condition is not met, it is possible that the SPC 4-2 will no longer recognize a frame.

11.4 Other Pins

11.4.1 Test Pins

Description

All output and I/O pins can be switched to the high-resistance state via a test pin XTEST0. To test the chip with test equipment (not in the target hardware environment!), an additional input (XTEST1) is provided. In conjunction with various other pins, this input allows the manufacturer to test the chip via a test bus. The interrupted memory (RAM and ROM) can also be tested. During operation, the test inputs must be connected to VDD.

11.4.2 XHOLDTOKEN

Description

This pin is not used in the compatibility mode but can be controlled with mode register 2, bit 0.

In the extended SPC 4-2 mode, an error triggered signal can be generated here for measurement purposes (depending on mode register 4, bits 5..4).

11.5 Interrupt Timing

Interrupts:

No.	Parameters	MIN	MAX	Unit
1	Interrupt-inactive time 48 periods of the SPC 4-2 clock (at 48 MHz = 1 µs)	1		µs

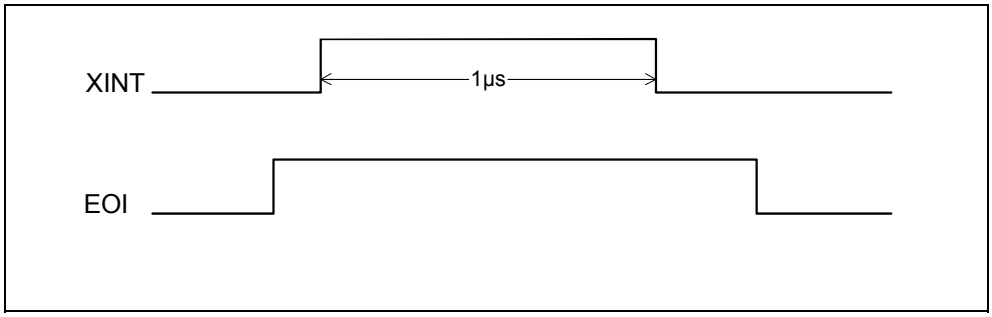

Figure 11-1 Interrupt Timing

11.6 Reset Timing

Description

To allow the SPC 4-2 to be reset correctly, it requires a pulse of at least 100 ns duration.

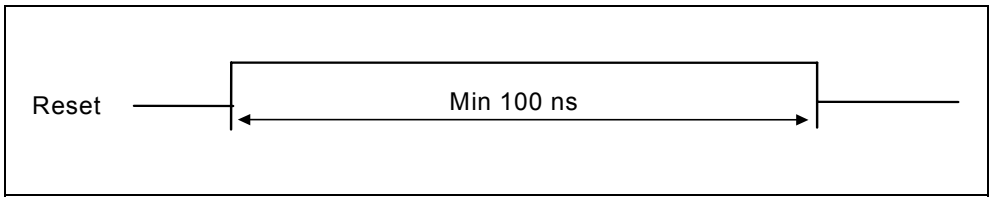

Figure 11-2 Reset Timing

11.7 Intel /Siemens 8051 (synchronous) etc.

11.7.1 Circuit Diagram

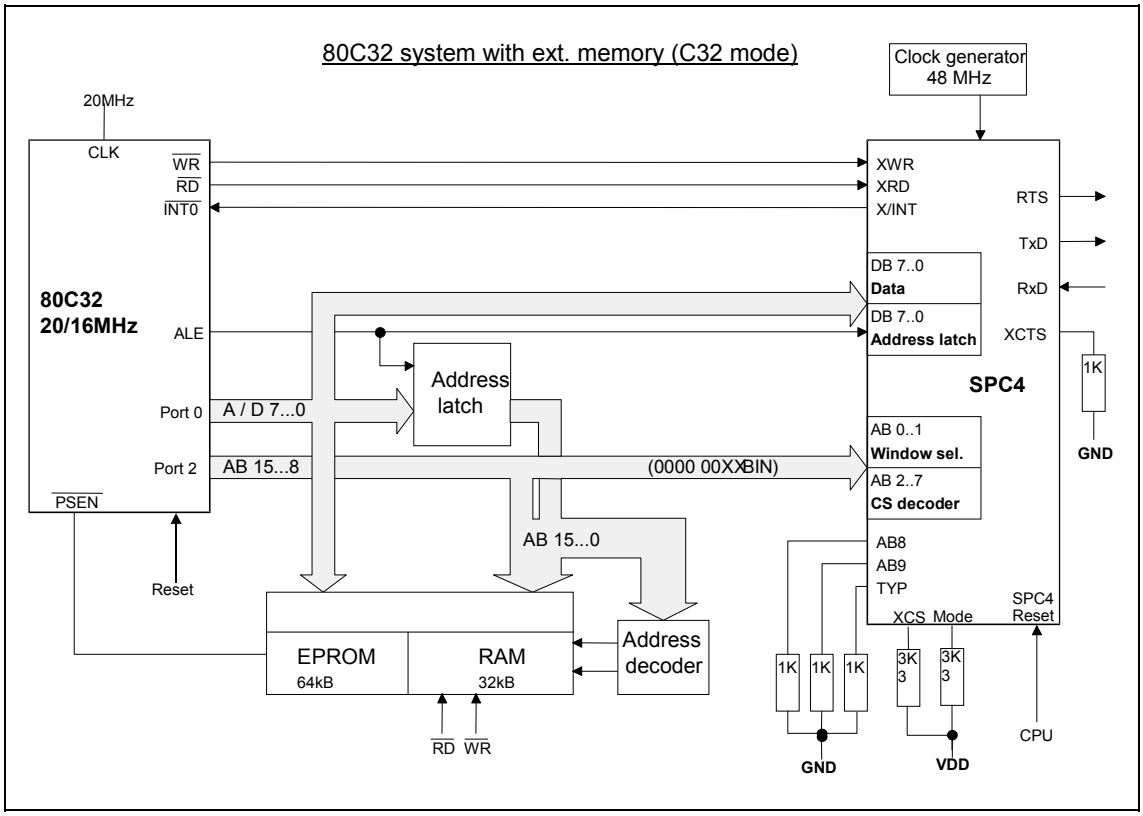

Figure 11-3 Circuit Diagram

Typ Mode 0 1 (synchronous INTEL)	INTEL, CPU Basis 80C51/2 (80C32), microcontrollers from various vendors • Synchronous (rigid) bus; timing without evaluation of the READY signal • 8-bit multiplexed bus ADB(7-0), The following can be connected: • Microcontroller families, e.g. INTEL, SIEMENS, PHILIPS ... Address decoder on the SPC 4-2 is activated; CS signal is supplied internally: • The lower address bits A(7-0) are stored in an internal address latch with the ALE signal. On the SPC 4-2 , the internal CS decoder is activated and generates its own CS signal from the addresses A(9-0). • The integrated address decoder is hardwired so that the SPC 4-2 must always be addressed at the fixed address at A(7...0)=0000 00xxb , and the SPC 4-2 selects the corresponding address window from the signals A(1,0) . • In this mode, the CS pin (XCS) must be connected to VDD (high potential) Wiring: Connection diagrams are stipulated by the specification. • ADB(7-0) to SPC 4-2 pin DB(7-0), AB(15-8) to SPC 4-2 pin • AB(7-0) and SPC 4-2 pin AB (9,8) connected to VSS.

11.7.2 Timing 80C32

In this mode, all accesses are started by the falling edge at XRD or XWR.

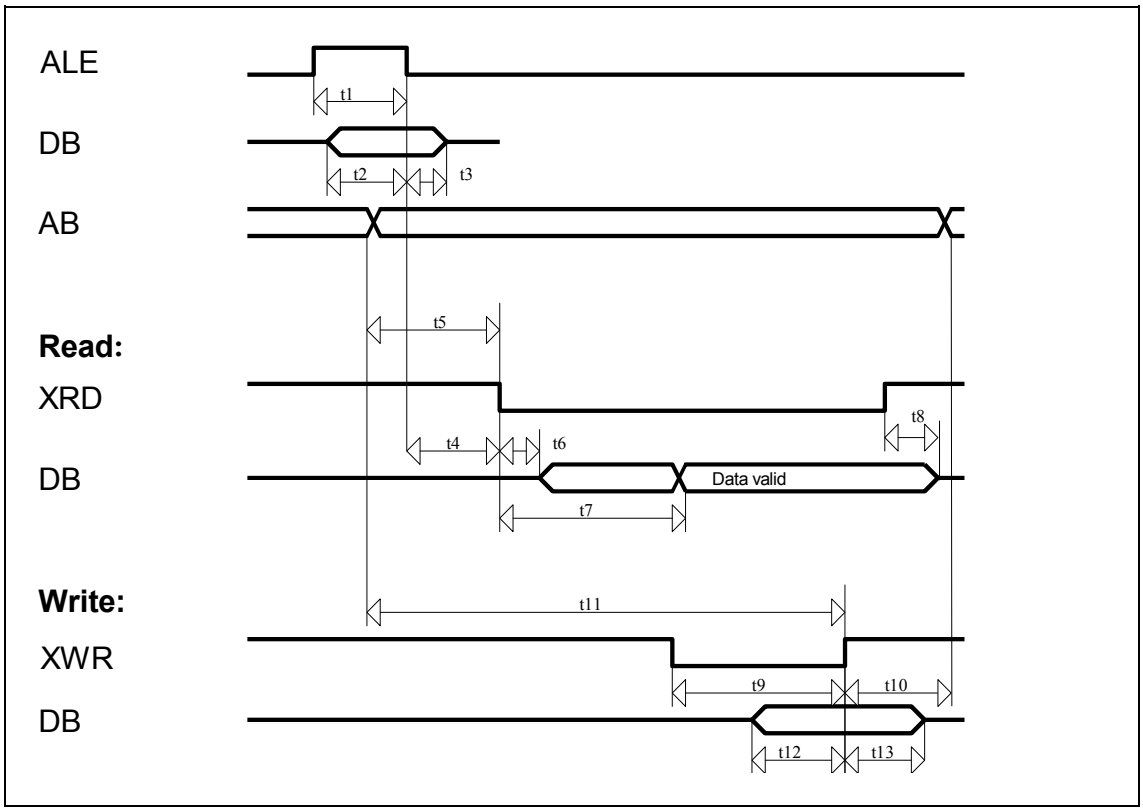

Figure 11-4 Timing 80C32

Bus Interface Timing Intel Synchronous

		Min.	Max.	Unit
t_1	ALE pulse width	10		ns
t_2	Setup time DB before ALE↓	5 (8)		ns
t_3	Hold time DB after ALE↓	8 (12)		ns
t_4	ALE↓ to XRD↓	20 (30)		ns
t_5	Setup time AB before XRD↓	20 (30)		ns
t_6	XRD↓ until DB low resistance		18 (27)	ns
t_7	Access time of XRD↓ until DB valid		$T_{SPC\ 4\text{-}2}$ + 52 (77)	ns
t_8	XRD↑ until DB high resistance		18 (27)	ns
t_9	XWR pulse width	10		ns
t_{10}	Hold time AB compared with XWR↑	0		ns
t_{11}	AB to XWR↑	20 (30)		ns
t_{12}	Setup time DB before XWR↑	10 (15)		ns
t_{13}	Hold time DB after XWR↑	5 (8)		ns

Table 11-5: Bus Interface Timing Intel Synchronous

Times in brackets apply for 3.3 V. For write timing, note the information in Section 11.3.

11.8 Intel X86 (asynchronous)

11.8.1 Circuit Diagram

In the X86 mode, the X86 bit must be set in mode register 2.

If the **SPC 4-2 is connected to a 80286** or similar, remember that the processor access words. This means that either a swapper is required that switches the relevant characters from the SPC 4-2 to the corresponding byte position of the 16-bit data bus when data are read or the lower address bit is not connected and the 80286 accesses words and only the lower byte is evaluated as shown in the diagram.

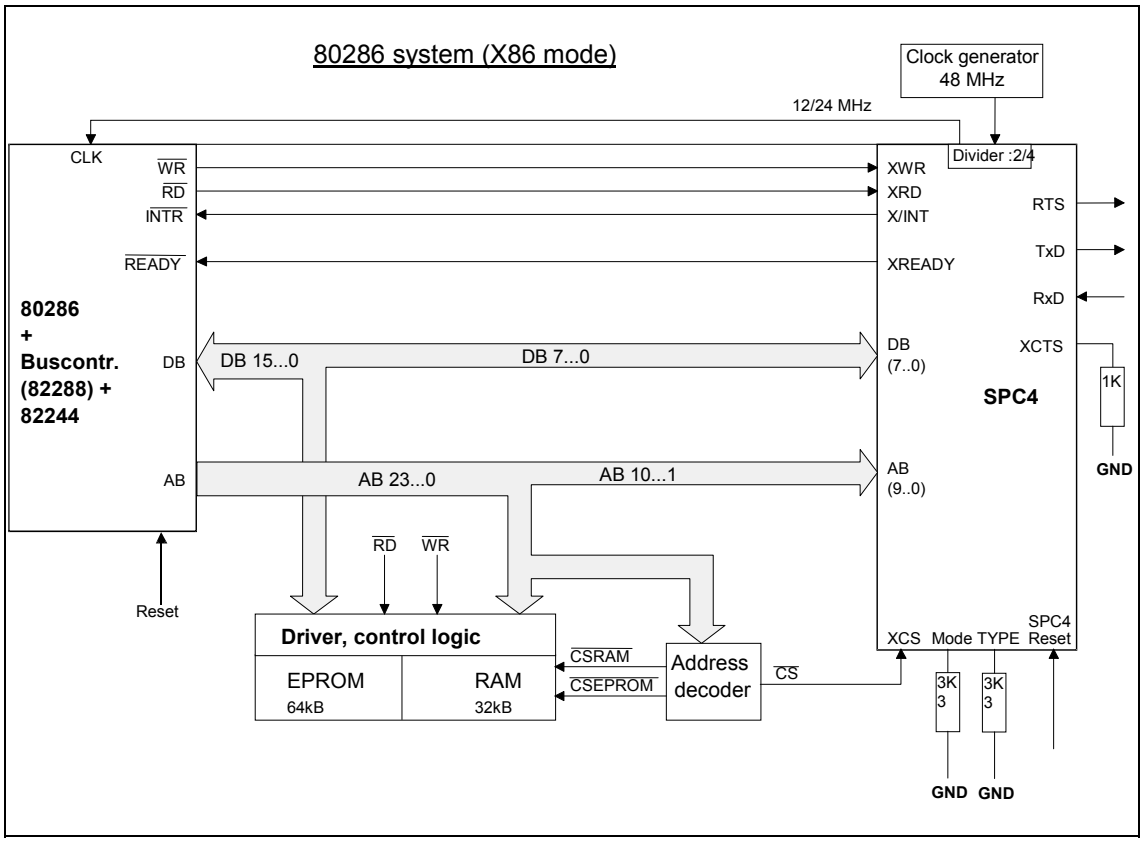

Figure 11-6 Circuit Diagram

Typ Mode 0 0 (asynchronous INTEL)	INTEL and SIEMENS 16-/8-bit microcontroller families • Asynchronous bus; timing with evaluation of the XREADY signal • 8-bit non-multiplexed bus: DB(7-0); AB(9-0) The following can be connected: • Microcontroller families, e.g. SIEMENS, 80C16x and INTEL X86 **The address decoder is deactivated on the SPC 4-2; CS signal is supplied to the SPC 4-2:** • External address decoding is always required • External chip-select logic if this does not exist on the microcontroller Note: Bit X86 in mode register 2 must be set for this mode.

11.8.2 Timing x86

In this mode, all accesses are triggered by the falling edge at XRD or XWR. The ALE input can adopt any values since it is disabled internally.

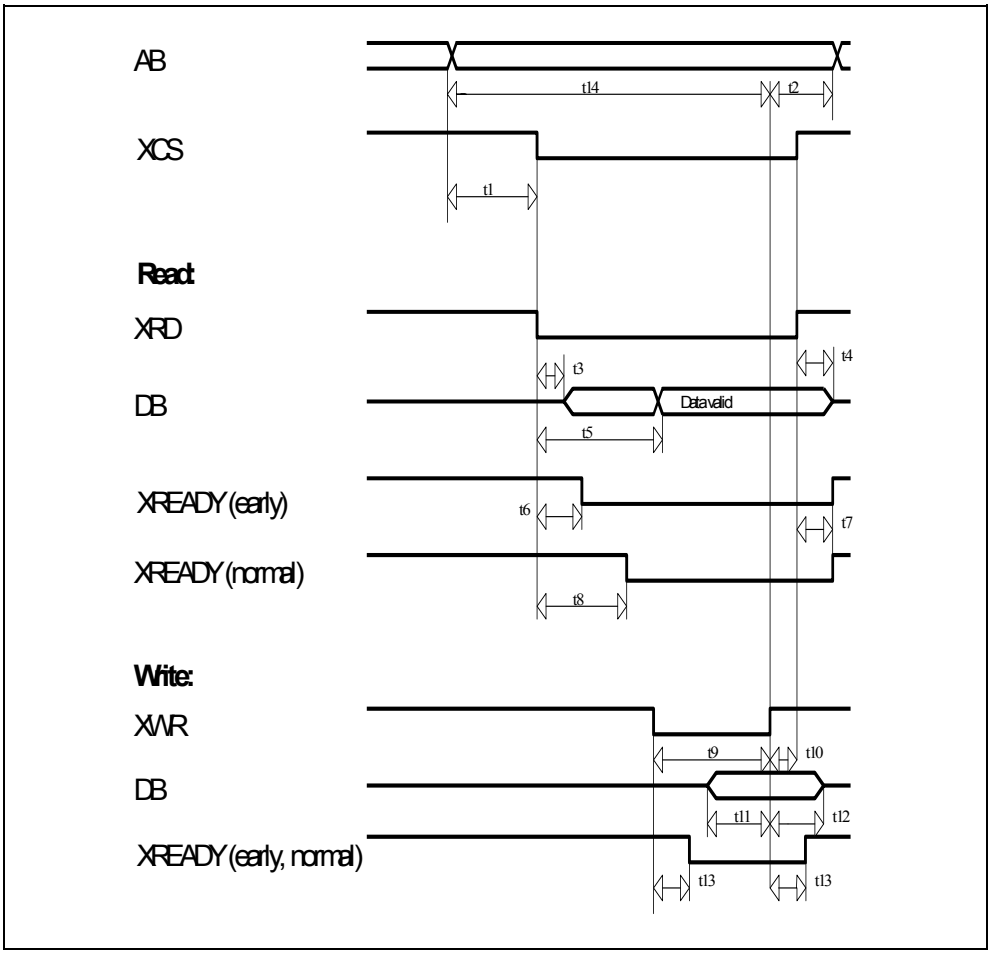

Figure 11-7 Bus Interface Timing Intel Asynchronous (X86)

		Min.	Max.	Unit
t_1	Setup time AB before XRD↓ and XCS↓ active	20 (30)		ns
t_2	Hold time AB after XWR↑	0		ns
t_3	XCS, XRD↓ until DB low resistance		18 (27)	ns
t_4	XCS, XRD↑ until DB high resistance		18 (27)	ns
t_5	Access time of XRD↓ until data valid		$T_{SPC\ 4\text{-}2}$ + 52 (77)	ns
t_6	**XCS, XRD↓ until XREADY↓ (early)**	0	$T_{SPC\ 4\text{-}2}$+ 18 (27)	ns
t_7	XCS, XRD↑ until XREADY↑ (early, normal)	0	17 (26)	ns
t_8	XCS, XRD↓ until XREADY↓ (normal)	$T_{SPC\ 4\text{-}2}$	2 $T_{SPC\ 4\text{-}2}$ + 18 (27)	ns
t_9	Pulse width XWR	10		ns
t_{10}	Hold time XCS after XWR↑	0		ns
t_{11}	Setup time DB before XWR↑	10 (15)		ns
t_{12}	Hold time DB after XWR↑	5 (8)		ns
t_{13}	XWR until XREADY (early, normal)	0	16 (24)	ns
t_{14}	Setup time AB before XWR↑	20 (30)		ns

Table 11-8: Bus Interface Timing Intel Synchronous

Times in brackets apply for 3.3 V. For write timing, note the information in Section 11.3.

11.9 Siemens 80C165 (asynchronous)

11.9.1 Circuit Diagram

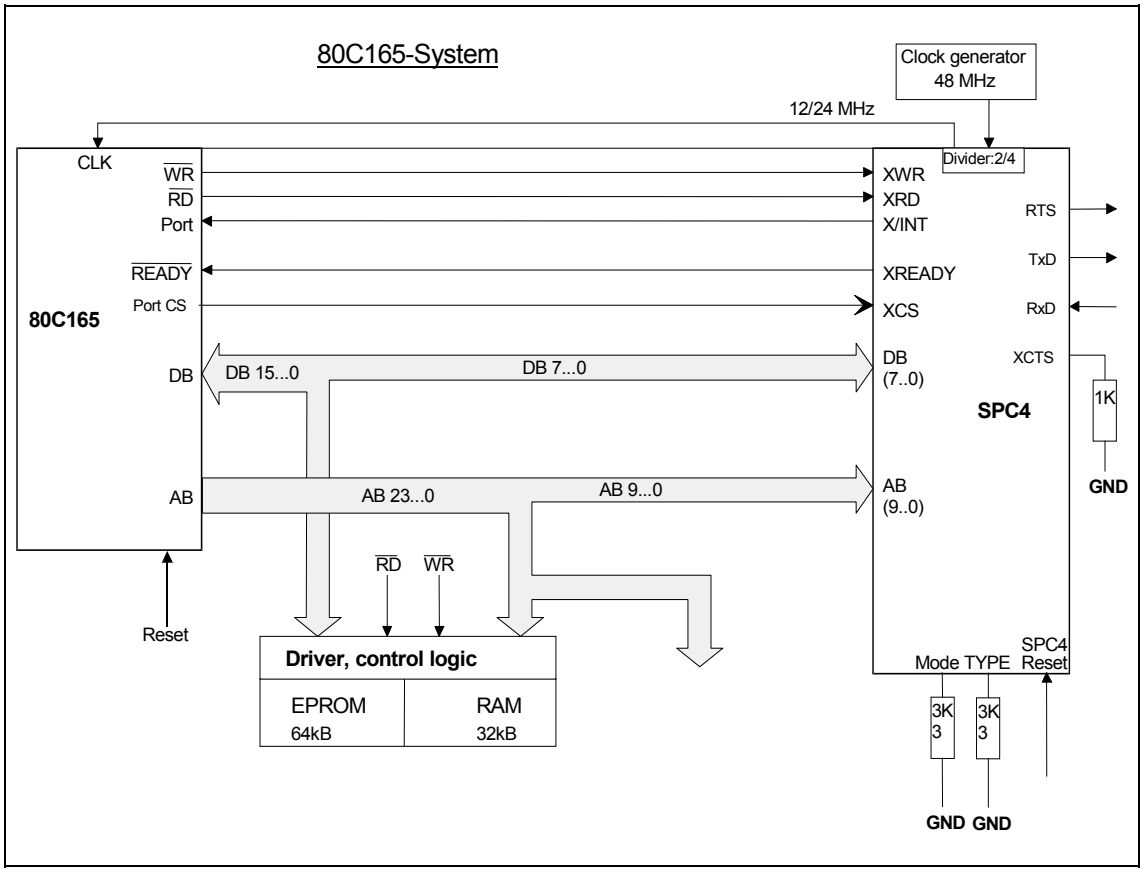

Figure 11-9 Circuit Diagram

Typ Mode	INTEL and SIEMENS 16-/8-bit microcontroller families • Asynchronous bus; timing with evaluation of the XREADY signal • 8-bit non-multiplexed bus: DB(7-0); AB(9-0) The following can be connected: • Microcontroller families, e.g. SIEMENS, 80C16x and INTEL X86 Address decoder on the SPC 4-2 is deactivated; CS signal is supplied to the SPC 4-2 • External address decoding is always required • External chip-select logic if this does not exist on the microcontroller Note: Bit X86 in mode register 2 must be set for this mode.
0 0 (asynchronous INTEL)	

11.9.2 Timing 80C165

Description

This mode is only reached when bit X86 is deleted in mode register 2 (X86 =0). Although the required write access can be made immediately with 80C165 timing, a wait time of 5 $T_{SPC\ 4\text{-}2}$ must elapse before further access is possible. All later access is then started by a falling edge at ALE. The ALE high phase can shorter than the clock period $T_{SPC\ 4\text{-}2}$.

If the values T_4 and T_{16} for XRD and XWR are not adhered to in this mode, access begins only at the falling edge of XWR or XRD and the access times from the table for Intel asynchronous (X86) apply.

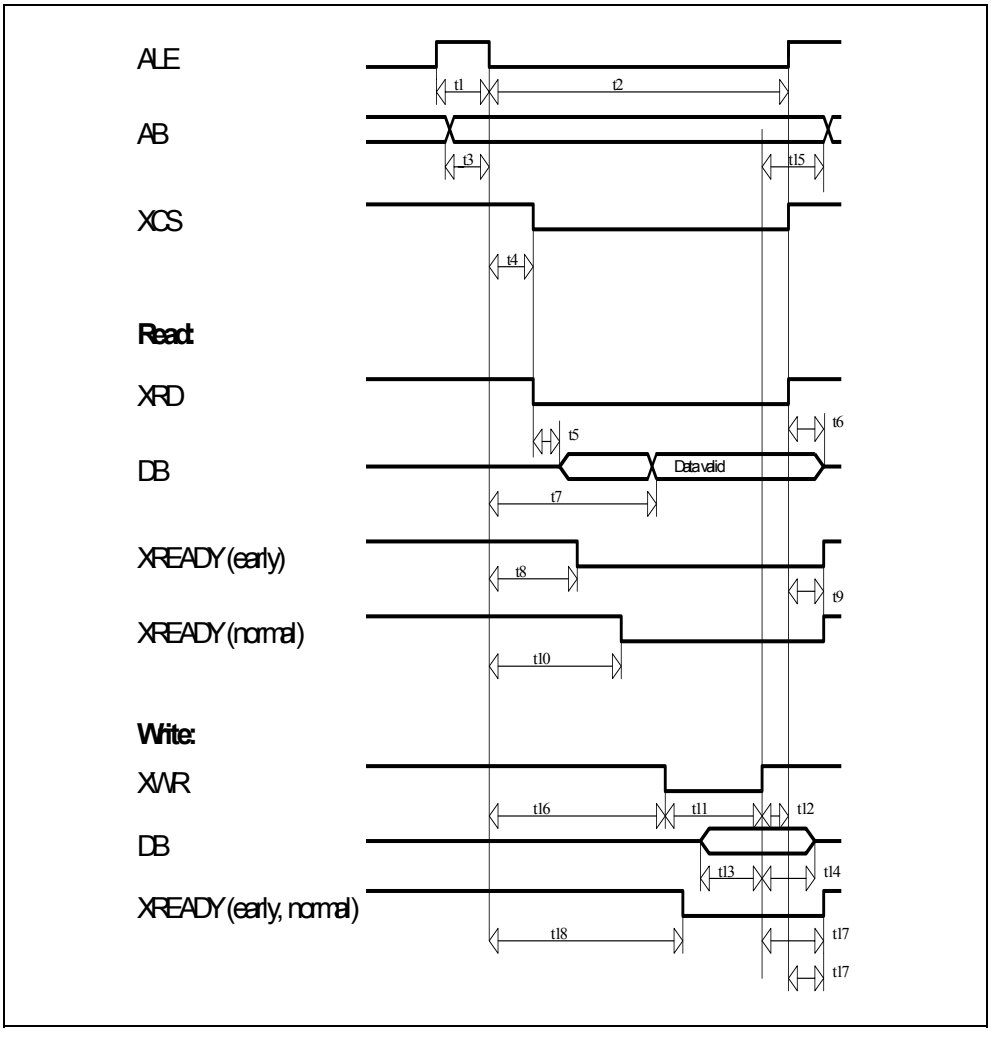

Figure 11-10 Timing 80C165

		Min.	Max.	Unit
t_1	ALE pulse width	10		ns
t_2	ALE low phase	5 $T_{SPC\ 4\text{-}2}$ -t_1		ns
t_3	Setup time AB before ALE↓	20 (30) - $T_{SPC\ 4\text{-}2}$		ns
t_4	XCS↓, XRD↓ to ALE ↓		$T_{SPC\ 4\text{-}2}$	ns
t_5	XCS↓, XRD↓ until DB low resistance		18 (27)	ns
t_6	XCS↑, XRD↑ until DB high resistance		18 (27)	ns
t_7	Access time of ALE↓ until data valid		2 $T_{SPC\ 4\text{-}2}$ + 52 (77)	ns
t_8	ALE↓ until XREADY↓ (early):	$T_{SPC\ 4\text{-}2}$ + 4 (6)	2 $T_{SPC\ 4\text{-}2}$ + 18 (27)	ns
t_9	XRD↑, XCS↑, ALE↑ until XREADY↑ (early, normal)		17 (26)	ns
t_{10}	ALE↓ until XREADY↓ (normal)	2 $T_{SPC\ 4\text{-}2}$ + 4 (6)	3 $T_{SPC\ 4\text{-}2}$ + 18 (27)	ns
t_{11}	Pulse width XWR	10		ns
t_{12}	Hold time XCS after XWR↑	0		ns
t_{13}	Setup time DB before XWR↑	10 (15)		ns
t_{14}	Hold time DB after XWR↑	10 (15)		ns
t_{15}	Hold time AB after XWR↑	0		ns
t_{16}	XWR↓ after ALE↓		$T_{SPC\ 4\text{-}2}$	ns
t_{17}	XWR↑, XCS↑, ALE↑ until XREADY (early, normal)	0	16 (24)	ns
t_{18}	ALE↓ until XREADY↓ (early, normal)	$T_{SPC\ 4\text{-}2}$	2 $T_{SPC\ 4\text{-}2}$	ns

Table 11-11: Bus Interface Timing Intel Asynchronous (80C165)

Times in brackets apply for 3.3 V operating voltage. For write timing, note the information in Section 11.3.

11.10 Timing 68HC16 (asynchronous)

11.10.1 Timing 68HC16

In this mode, all accesses are started by a falling edge at AS.

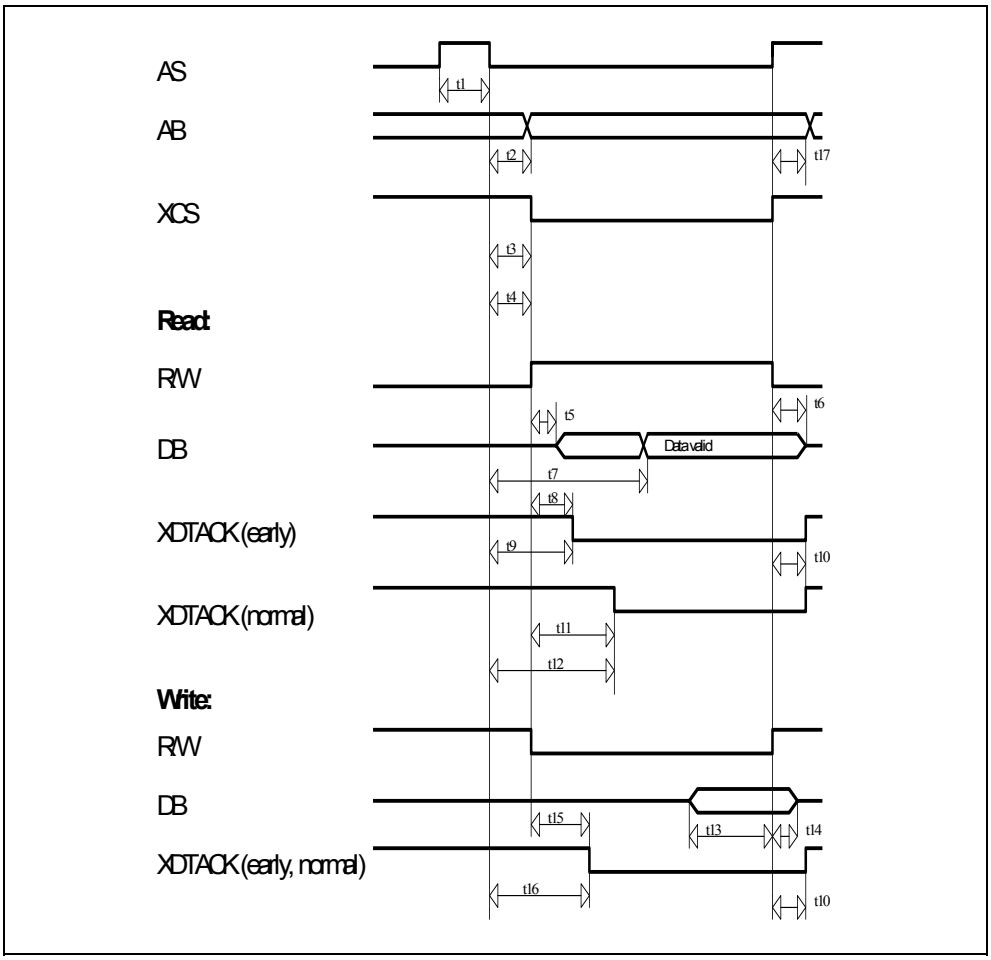

Figure 11-12 Bus Interface Timing Motorola Asynchronous

		Min.	Max.	Unit
t_1	Inactive time AS	10		ns
t_2	AS↓ until AB valid		2 $T_{SPC\ 4\text{-}2}$ - 20 (30)	ns
t_3	AS↓ until XCS↓		2 $T_{SPC\ 4\text{-}2}$ - 10 (15)	ns
t_4	AS↓ until R/W		$T_{SPC\ 4\text{-}2}$ - 10 (15)	ns
t_5	XCS↓, R/W↑ until DB low resistance		18 (27)	ns
t_6	XCS↑, R/W↓ until DB high resistance		18 (27)	ns
t_7	Access time of AS↓ until DB valid		3 $T_{SPC\ 4\text{-}2}$ + 52 (77)	ns
t_8	XCS↓, R/W↑ until XDTACK↓ (early)	0	$T_{SPC\ 4\text{-}2}$ + 18 (27)	ns
t_9	AS↓ until XDTACK↓ (early)	2 $T_{SPC\ 4\text{-}2}$	3 $T_{SPC\ 4\text{-}2}$ + 18 (27)	ns
t_{10}	AS↑ until XDTACK↑ (early, normal)	0	16 (24)	ns
t_{11}	XCS↓, RWX↑ until XDTACK↓ (normal)	$T_{SPC\ 4\text{-}2}$	2 $T_{SPC\ 4\text{-}2}$	ns
t_{12}	AS↓ until XDTACK↓ (normal)	3 $T_{SPC\ 4\text{-}2}$ + 4 (6)	4 $T_{SPC\ 4\text{-}2}$ + 18 (27)	ns
t_{13}	Setup time DB before AS↑	5 (8)		ns
t_{14}	Hold time DB after AS↑	12 (18)		ns
t_{15}	XCS↓ at XDTACK↓ (early, normal)		18 (27)	ns
t_{16}	AS↓ at XDTACK↓ (early, normal)	$T_{SPC\ 4\text{-}2}$	2 $T_{SPC\ 4\text{-}2}$ + 18 (27)	ns
t_{17}	Hold time AB after AS↑		10 (15)	ns

Table 11-13: Bus Interface Timing Motorola Asynchronous

Times in brackets apply for 3.3 V. For write timing, note the information in Section 11.3.

11.11 Motorola 68HC11 (synchronous)

11.11.1 Timing 68HC11

In this mode, access is started by a rising edge at E-clock. The clock rate of the SPC 4-2 (QCLK-IN) must be at least four times higher than that of the E-clock.

Note

If E-clock = 3 MHz, CLK must be 24 MHz.

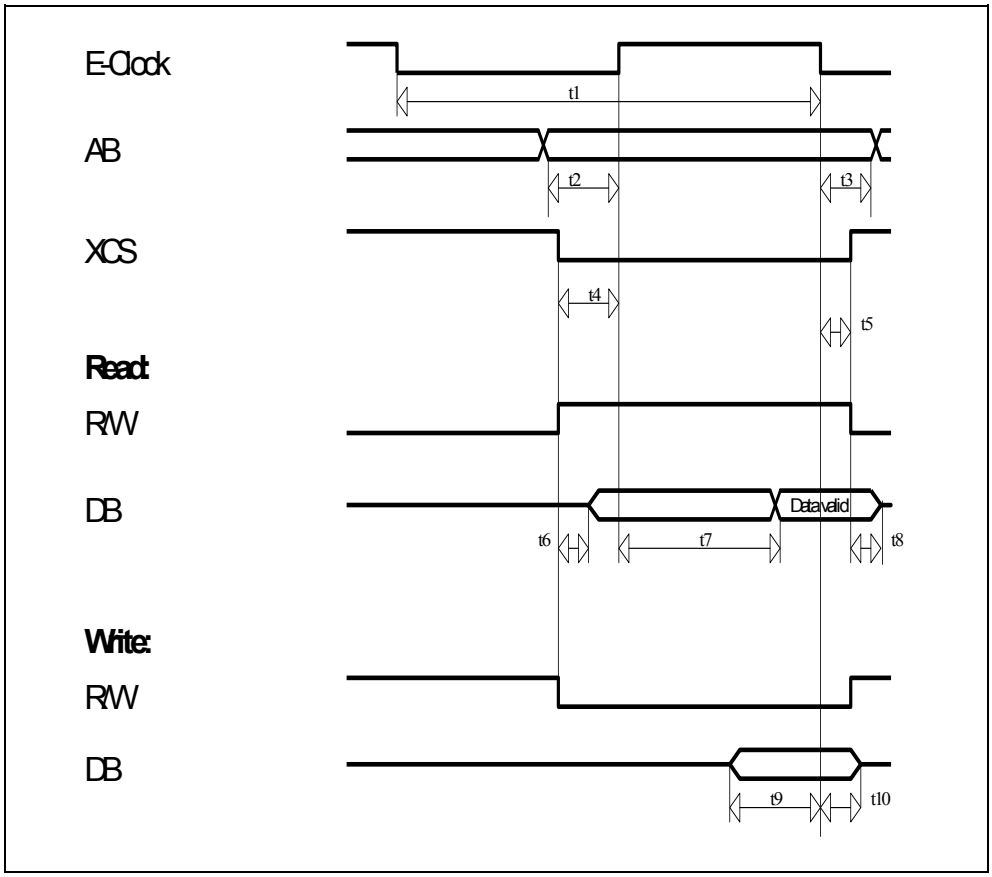

Figure 11-14 Timing 68HC11

		Min.	Max.	Unit
t_1	Period E-clock	333		ns
t_2	Setup time AB before E-clock↑	20 (30)		ns
t_3	Hold time AB after E-clock↓	15 (22)		ns
t_4	Setup time XCS, R/W E-clock↑	15 (22)		ns
t_5	Hold time XCS, R/W to E-clock↓	0		ns
t_6	XCS↓, R/W↑ until DB low resistance		18 (27)	ns
t_7	Access time of E-clock↑ until DB valid		$T_{SPC\ 4\text{-}2}$ + 57 (85)	ns
t_8	XCS↑, R/W↓ until DB high resistance		18 (27)	ns
t_9	Setup time DB before E-clock	10 (15)		ns
t_{10}	Hold time DB after E-clock	20 (30)		ns

Table 11-15: Bus Interface Timing Motorola Synchronous

Times in brackets apply for 3.3 V. For write timing, note the information in Section 11.3.

Technical Specifications

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12.1 Maximum Limit Values

Parameters	Meaning	Limits	Unit
DC supply voltage	VDD	-0.3 to 7.0	V
Input voltage	VI	-0.3 to VDD +0.3	V
Output voltage	VO	-0.3 to VDD +0.3	V
DC output current	IO	see table	mA
DC supply current	IDD, ISS	Approx. 60	mA
Ambient temperature	Topt	-40 to +85	°C
Storage temperature		TBD	
Power loss	Pmax	300	mW/5 V/12 Mbps
Power loss	Pmax	20	mW/3.3 V/31.25 Kbps

Table 12-1: Maximum Limit Values

Notice:
Operation over longer periods with these values reduces the service life.

12.2 Permitted Operating Values

Parameters	Meaning	MIN.	MAX.	Unit
DC supply voltage	VDD	4.5	5.5	V
(VSS=0V)				
DC supply voltage	VDD	3.0	3.6	V
(VSS=0V)				
Input voltage	VI	0	VDD	V
Input voltage (high level)	VIH	0.7 VDD	VDD	V
Input voltage (low level)	VIL	0	0.3 VDD	V
Output voltage	VO	0	VDD	V
Ambient temperature	TA	-40	+85	°C
DC supply current typically		55		5 V/12 Mbps
DC supply current typically		3.6		3.3 V/31.25 Kbps

Table 12-2: Permitted Operating Values

12.3 Power Consumption

The power consumption of a large-scale integrated digital module such as the SPC 4-2 depends to a great extent on the selected mode. The power supply, the external clock frequency, data transmission rate and type and frequency of access to the memory interface determine the current consumption of the chip. The information on the current consumption below can therefore only be a guideline and the actual values must be measured in each individual case.

Power supply VDD = 5 V (with the exception of the information in the bottom line where VDD = 3.3 V)

All information on current consumption in [mA]

Clock Frequency / Mode	2 MHz	4 MHz	8 MHz	24 MHz	48 MHz
Reset	0.25	0.7	1.4	2.9	5
Memory Access	4	7	11	23	43
Data exchange 9.6 Kbps	5.4	-	-	-	-
Data exchange 19.2 Kbps	-	4.5	-	-	-
Data exchange 500 Kbps	-	5.5	-	-	32
Data exchange 1.5 Mbps	-	-	-	-	38
Data exchange 12 Mbps	–	–	–	–	55
Data exchange 31.25 Kbps VDD = **3.3 V**	3.6	–	–	–	–

Table 12-3: Current Consumption

The values shown in the table are typical values obtained by measurement on several chips in various modes:

- Reset
  RESET input active, chip is in the reset status

- Memory access
  The connected CPU reads and writes the SPC 4-2 internal RAM cyclically.

- Data exchange
  The SPC 4-2 is in the data exchange status, an external master exchanges data with the slave cyclically. The input/output data is read from or written to the SPC 4-2 memory cyclically by the connected CPU.

12.4 DC Specification of the Pad Cells

Parameters	NAME	MIN.	Type	MAX.	Unit
Threshold voltage 0 level	V+	0		1.8	V
Schmitt trigger at 3.3 V					
Threshold voltage 1 level	V-	0.7		VDD	V
Schmitt trigger at 3.3 V					
Threshold voltage 0 level	V+	0		3.7	V
Schmitt trigger at 5.0 V					
Threshold voltage 1 level	V-	1.5		VDD	V
Schmitt trigger at 5.0 V					
Input leakage current	II			1	uA
Output leakage current	IOZ			10	uA
Output current 0 level	IOL	4		(1)	mA
4 mA cell					
Output current 1 level	IOH	-4		(2)	mA
4 mA cell					
Output current 0 level	IOL	10		(1)	mA
10 mA cell					
Output current 1 level	IOH	-10		(2)	mA
10 mA cell					
Short-circuit current	IOS			TBD(3)	mA
Input capacitance	CIN		5		pF
Output capacitance	COUT		5		pF
I/O capacity	CI/O		5		pF

(1) VOL = 0.5 V
(2) VOH = VDD-0.5 V
(3) at < s.

Table 12-4: Pad Cells

12.5 Ratings of the Output Drivers

Signal line	Direction	Driver type	Driver strength	Cap. load	Pullup
DB 0-7	I/O	Tristate	4 mA	50 pF	min. 50 kΩ
RTS-ADD	L	Tristate	4 mA	50 pF	
TxD	O	Tristate	4 mA	50 pF	
X/INT	L	Tristate	4 mA	50 pF	
X/INTCI	L	Tristate	4 mA	50 pF	
XREADY	L	Tristate	10 mA	50 pF	
XHOLD-TOKEN	L	Tristate	4 mA	50 pF	
ISCLK-Out	L	Tristate	10 mA	50 pF	

Table 12-5: Ratings of the Output Drivers

Package

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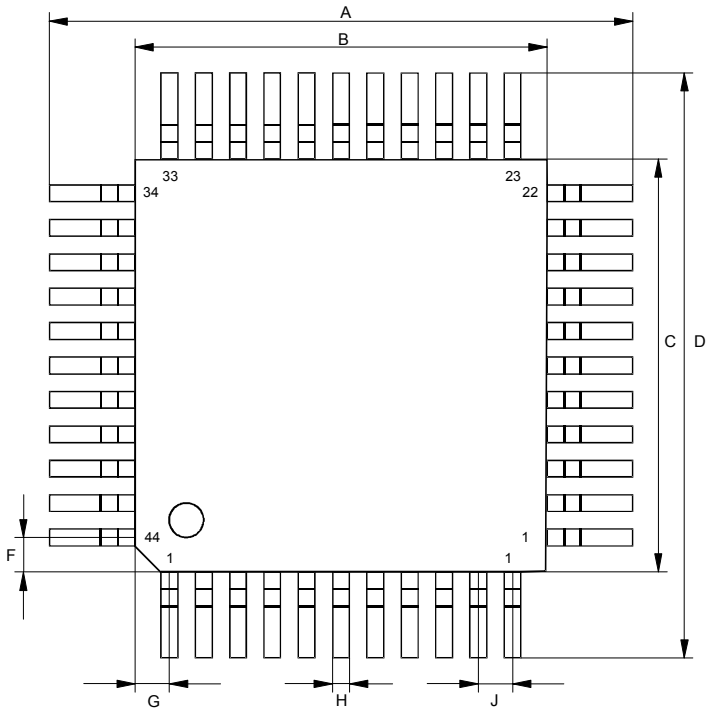

A = 12.0 ±0.2 mm
B = 10.0 ±0.2 mm
C = 10.0 ±0.2 mm
D = 12.0 ±0.2 mm
F = typ. 1.0 mm
G = typ. 1.0 mm
H = 0.37 ±0.08 mm
J = 0.8 mm
L = 0.6 ±0.15 mm
M = 0.15 ±0.05 mm (pin thickness)
P = 1.4 ±0.15 mm
θ = 0° to 10°
R = max. 1.6 mm
S = 0.1 ±0.05 mm

Figure 13-1 44-Pin LQFP Package

13.1 Instructions on Handling

Warning

When handling and working with electronic components, make sure that you keep to the **ESD guidelines** .

Warning

The **SPC 4-2** is a **component subject to cracking**, and must be handled accordingly.

- Before working on the SPC 4-2 it must be dried if the chip has been stored for more than 48 hours without being in a dry pack.
- In this case, the component must then be dried **at 125 ^{O}C for 24 hours** and then **processed within 48 hours**. Due to the solderability of the component, it can only undergo this drying process once.
- Care must also be taken to be sure that the connectors of the SPC 4-2 are not bent. Problem-free processing can only be guaranteed when coplanarity of the pins of less than 0.1 mm before fitting to the board is ensured.
- Infrared soldering with the solder profile according to CECC00802 has been approved for the SPC 4-2.

- Lead Finish: Sn-Ag
- During lead-free infrared soldering, the maximum temperature 260 °C must not be exceeded on the package surface and the temperature must not exceed 230 °C for a period longer than 30 to 50 seconds.

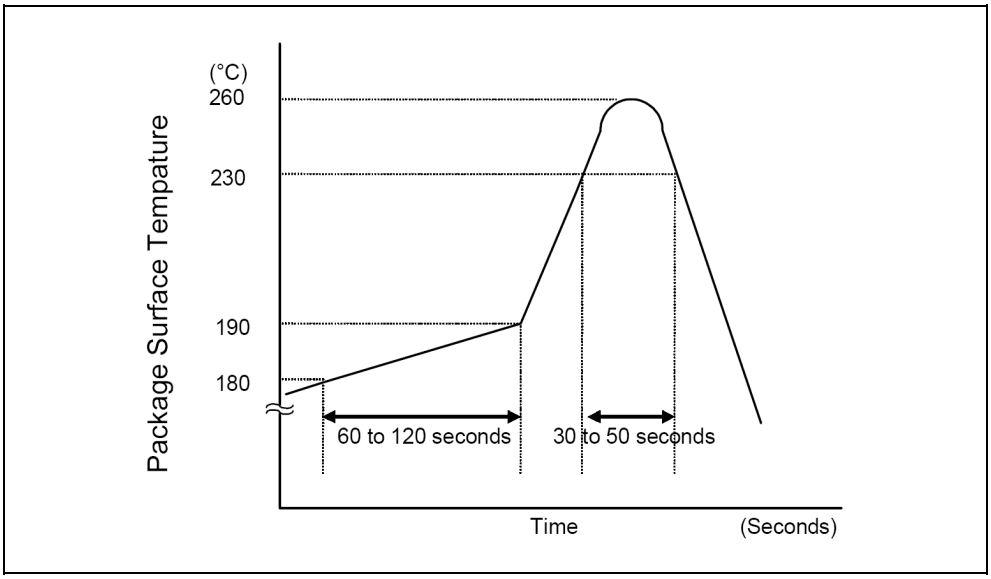

Figure 13-2 Example of a temperature profile

13.2 Labeling

The labeling of the SPC 4-2 LF contains the following information as shown symbolically Figure 13-3:

Manufacturer:	Siemens AG
Type name:	SPC 4-2 LF
Type code:	company internal code; 190C580EF003
Production information:	coded production identifier allowing a batch to be identified if faults are discovered.

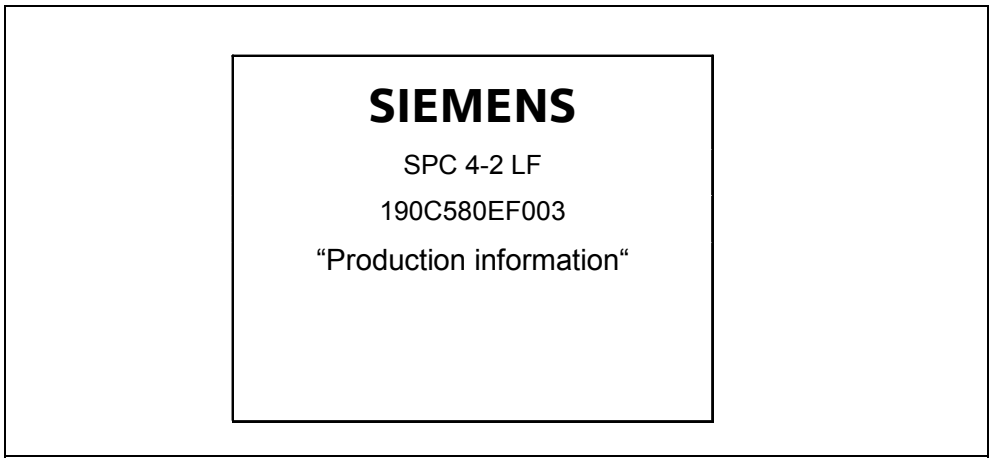

Figure 13-3 Printing the SPC 4-2 LF

13.3 Packaging of the ASIC

The SPC 4-2 ASICs ship in two different types of packaging:

- Small pack (pack of 5)
- Single Tray (pack of 160)

Box

This type of packing is suitable for laboratories. Since the positioning is not reproducible, this is not suitable for automatic assembly.

Tray

The tray is suitable for automatic assembly. The dimensions are shown in Figure 13-4.

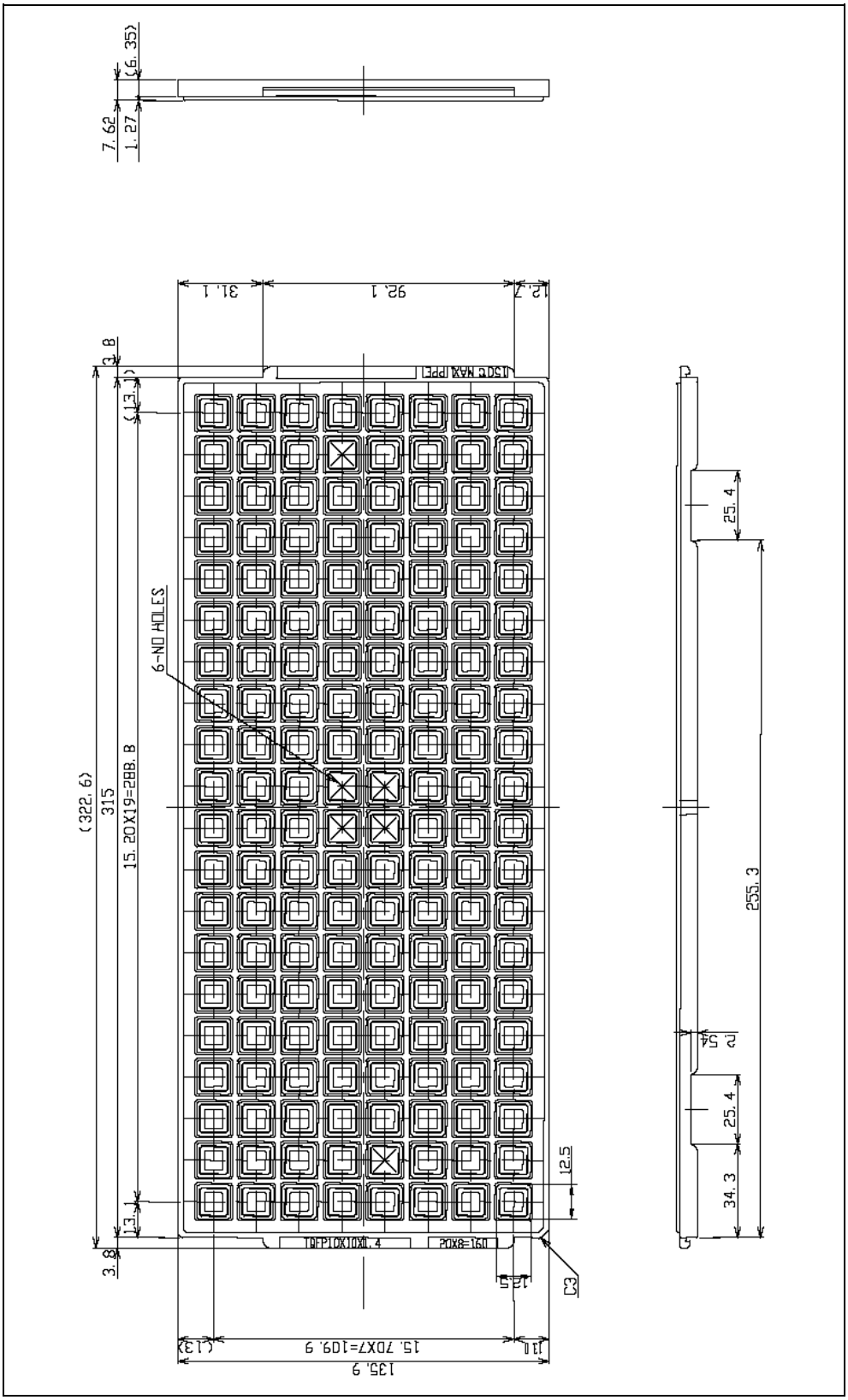

Figure 13-4 Tray Spezification

References

14

- DIN 19245 Part 1 (Beuth-Verlag)
- DIN 19245 Part 2 (Beuth-Verlag)
- DIN E 19245 Part 3 (Beuth-Verlag)
- PNO Guidelines PROFIBUS-PA (PNO)
- EN50170 Volume 2
- IEC 61158:2000 Part 2, 3, 4, 5, 6

Addresses

15

15.1 PNO

PROFIBUS User Organization
Head Office
Haid- und Neu- Straße 7
76131 Karlsruhe
Germany
Tel.: (0721) 9658-590
Fax.: (0721) 9658-589

15.2 Contacts in the Interface Center

Siemens AG
ComDeC

Correspondence to:
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90713 Fürth

House address:
Würzburgerstr.121
90766 Fürth

Tel.: (0911) 750 – 2080
Fax: (0911) 750 – 2100

E-mail:
ComDeC@fthw.siemens.de

Appendix 16

16.1 Server Software for the SPC 4-2

Figure 16-1 and Figure 16-2 show the basic structure.

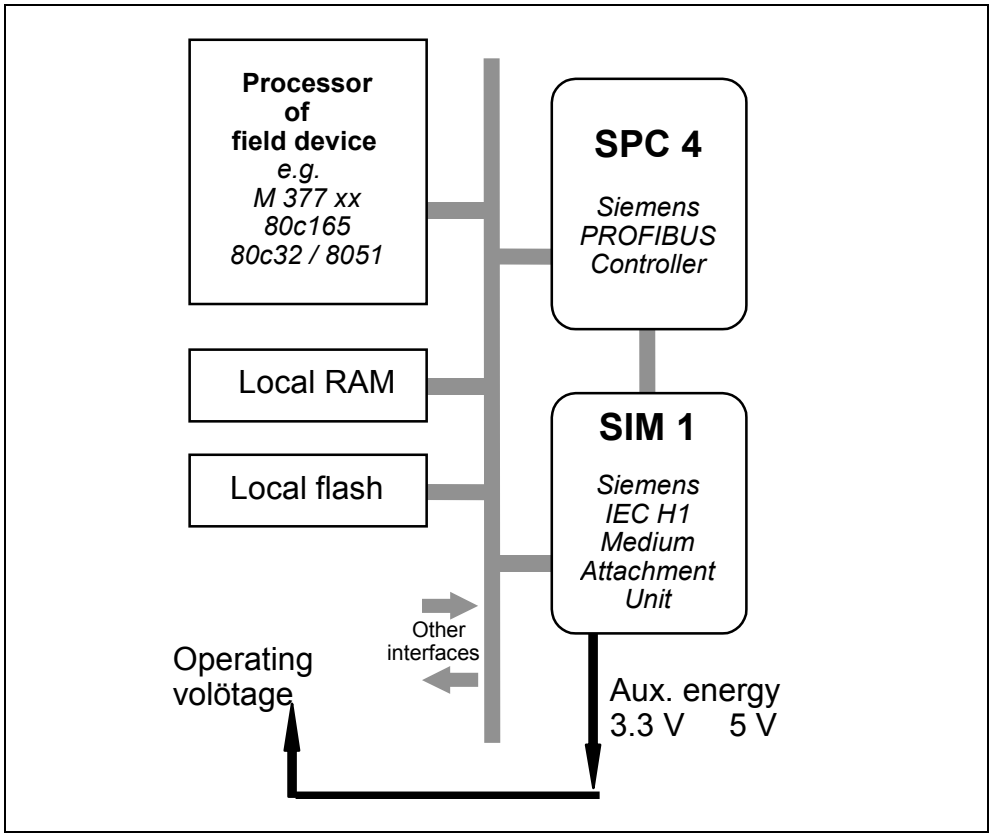

Figure 16-1 Hardware Architecture with SIM 1/SPC 4-2 with auxiliary energy decoupling (at constant current consumption additional 6.6 V)

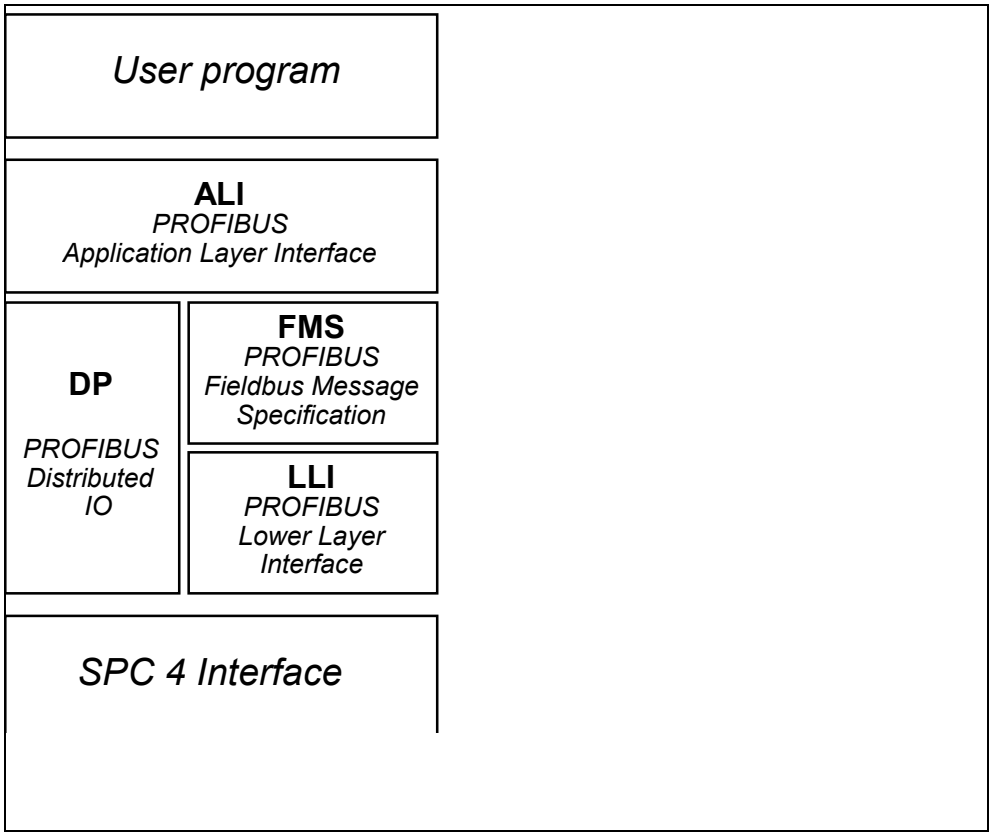

Figure 16-2 System Environment of the PROFIBUS PA/FMS/DP Server Software

Suitable server software is available from the SIMATIC NET Provider, TMG.

16.2 SIM1

Description

The ASIC SIM 1 supplements the ASIC line for the ASIC SPC 4-2 and DCP 31 protocol.

The communication interface chip SIM 1 is intended for use in the intrinsically safe fieldbus systems at 31.25 Kbps and implements the functions of a Medium Attachment Unit for IEC H1 (identical with the PROFIBUS PA and Foundation Fieldbus□) in compliance with IEC 61158-2.

Only a few external components are required in addition to the ASIC SIM 1 to connect modules or field devices to an intrinsically safe network for PROFIBUS PA and FF.

In conjunction with the SPC 4-2 (the Siemens PROFIBUS controller for slave applications), the functions of a PROFIBUS and FF slave can be handled optimally from the physical attachment to the communication control.

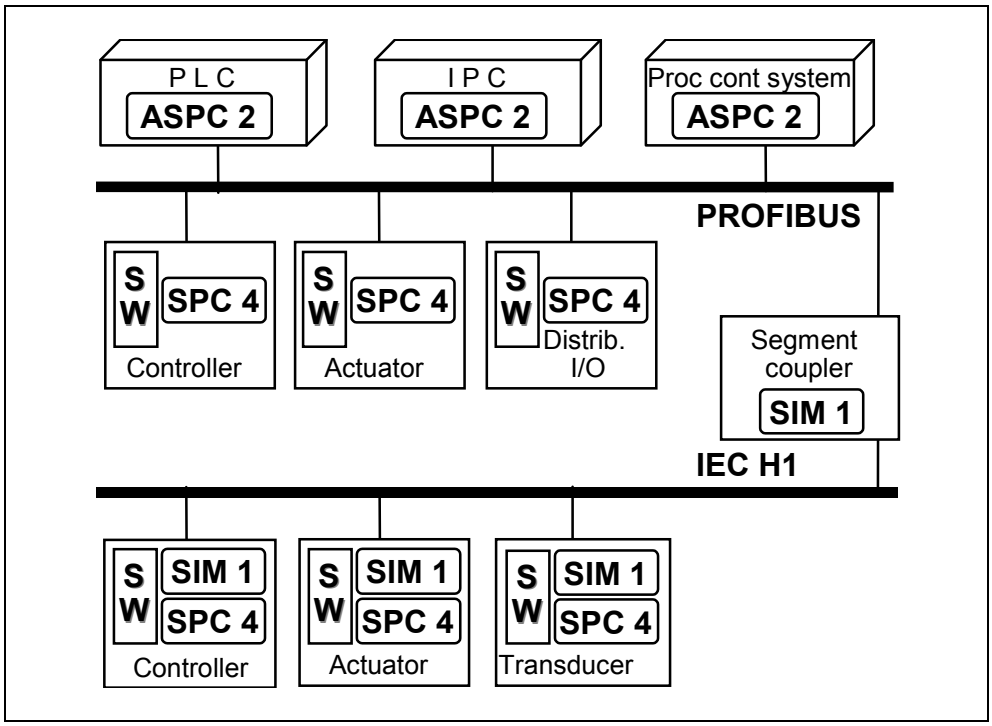

Figure 16-3 Environment of the ASIC

The following picture shows one possible way of attaching the SPC 4-2 to the ASIC SIM 1.

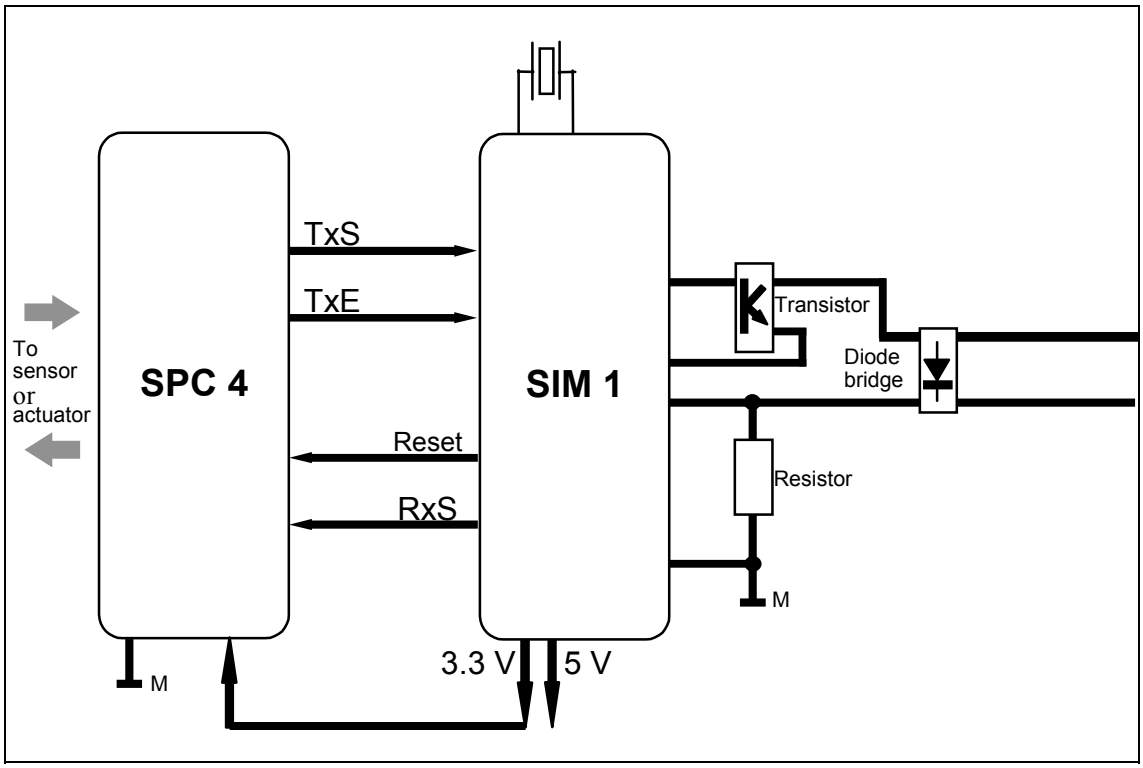

Figure 16-4 Application Example

SIM 1 in the constant current mode with SPC 4-2 without electrical isolation

- ❑