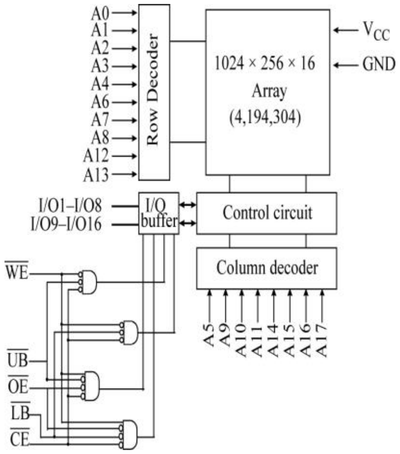
August 2004 **AS7C34098A**

3.3 V 256 K × 16 CMOS SRAM

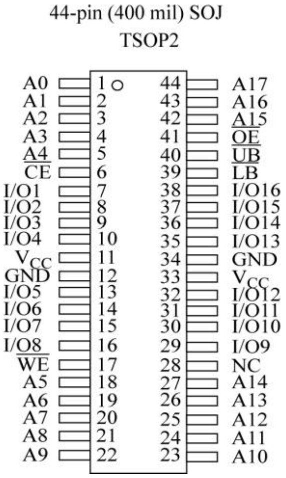
Features

- Pin compatible with AS7C34098
- Industrial and commercial temperature
- Organization: 262,144 words × 16 bits
- Center power and ground pins
- High speed
  - 10/12/15/20 ns address access time
  - 4/5/6/7 ns output enable access time
- Low power consumption: ACTIVE
  - 650 mW /max @ 10 ns
- Low power consumption: STANDBY
  - 28.8 mW /max CMOS
- Individual byte read/write controls
- Easy memory expansion with $\overline{\text{CE}}$, $\overline{\text{OE}}$ inputs
- TTL- and CMOS-compatible, three-state I/O
- JEDEC standard packages
  - 44-pin SOJ -400-mil
  - 44-pin TSOP 2
  - 48-pin Mini BGA
- ESD protection ≥ 2000 volts
- Latch-up current ≥ 200 mA

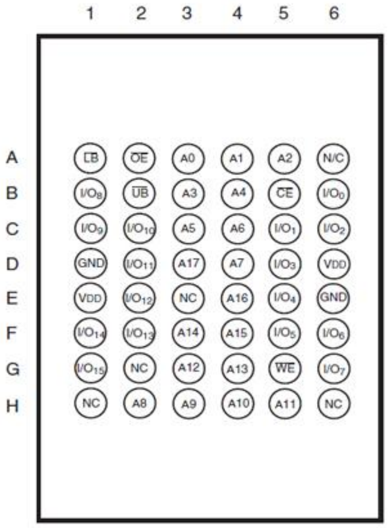
Logic block diagram



Pin arrangement for SOJ and TSOP 2



Bottom View 48BGA



Selection guide

		–10	–12	–15	–20	Unit
Maximum address access time		10	12	15	20	ns
Maximum output enable access time		4	5	6	7	ns
Maximum operating current	Industrial	180	160	140	110	mA
	Commercial	170	150	130	100	mA
Maximum CMOS standby current		8	8	8	8	mA

Functional description

The AS7C34098A is a high-performance CMOS 4,194,304-bit Static Random Access Memory (SRAM) device organized as 262,144 words × 16 bits. It is designed for memory applications where fast data access, low power, and simple interfacing are desired.

Equal address access and cycle times (t_{AA}, t_{RC}, t_{WC}) of 10/12/15/20 ns with output enable access times (t_{OE}) of 4/5/6/7 ns are ideal for high-performance applications. The chip enable input $\overline{CE}$ permits easy memory expansion with multiple-bank memory systems.

When $\overline{CE}$ is high the device enters standby mode. The device is guaranteed not to exceed 28.8mW power consumption in CMOS standby mode. A write cycle is accomplished by asserting write enable ($\overline{WE}$) and chip enable ($\overline{CE}$). Data on the input pins I/O1–I/O16 is written on the rising edge of $\overline{WE}$ (write cycle 1) or $\overline{CE}$ (write cycle 2). To avoid bus contention, external devices should drive I/O pins only after outputs have been disabled with output enable ($\overline{OE}$) or write enable ($\overline{WE}$).

A read cycle is accomplished by asserting output enable ($\overline{OE}$) and chip enable ($\overline{CE}$), with write enable ($\overline{WE}$) high. The chip drives I/O pins with the data word referenced by the input address. When either chip enable or output enable is inactive, or write enable is active, output drivers stay in high-impedance mode.

The device provides multiple center power and ground pins, and separate byte enable controls, allowing individual bytes to be written and read. $\overline{LB}$ controls the lower bits, I/O1–I/O8, and $\overline{UB}$ controls the higher bits, I/O9–I/O16.

All chip inputs and outputs are TTL- and CMOS-compatible, and operation is for 3.3V (AS7C34098A) supply. The device is available in the JEDEC standard 400-mil, 44-pin SOJ, TSOP 2.

Absolute maximum ratings

Parameter	Symbol	Min	Max	Unit
Voltage on V_{CC} relative to GND	V_{t1}	–0.50	+5.0	V
Voltage on any pin relative to GND	V_{t2}	–0.50	V_{CC} +0.50	V
Power dissipation	P_D	–	1.5	W
Storage temperature (plastic)	T_{stg}	–65	+150	°C
Ambient temperature with V_{CC} applied	T_{bias}	–55	+125	°C
DC current into outputs (low)	I_{OUT}	–	±20	mA

Note: Stresses greater than those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Truth table

CE	WE	OE	LB	UB	I/O1–I/O8	I/O9–I/O16	Mode
H	X	X	X	X	High Z	High Z	Standby (I_{SB}, I_{SB1})
L	H	H	X	X	High Z	High Z	Output disable (I_{CC})
L	X	X	H	H			
L	H	L	L	H	D_{OUT}	High Z	Read (I_{CC})
			H	L	High Z	D_{OUT}	
			L	L	D_{OUT}	D_{OUT}	
L	L	X	L	H	D_{IN}	High Z	Write (I_{CC})
			H	L	High Z	D_{IN}	
			L	L	D_{IN}	D_{IN}	

Key: X = Don't care, L = Low, H = High.

Recommended operating conditions

Parameter		Symbol	Min	Typical	Max	Unit
Supply voltage		V_{CC} (10/12/15/20)	3.0	3.3	3.6	V
Input voltage		V_{IH}^{**}	2.0	–	V_{CC} + 0.5	V
		V_{IL}^{*}	–0.5	–	0.8	V
Ambient operating temperature	commercial	T_A	0	–	70	°C
	industrial	T_A	–40	–	85	°C

* V_{IL} min = –1.0V for pulse width less than 5ns.

* V_{IH} max = V_{CC} + 2.0V for pulse width less than 5ns.

DC operating characteristics (over the operating range)[1]

Parameter	Symbol	Test conditions		–10		–12		–15		–20		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
Input leakage current	$\|I_{LI}\|$	V_{CC} = Max V_{IN} = GND to V_{CC}		–	1	–	1	–	1	–	1	µA
Output leakage current	$\|I_{LO}\|$	V_{CC} = Max $\overline{CE}$ = V_{IH} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL} $V_{I/O}$ = GND to V_{CC}		–	1	–	1	–	1	–	1	µA
Operating power supply current	I_{CC}	V_{CC} = Max $\overline{CE} \leq V_{IL}$, $f = f_{max}$ I_{OUT} = 0mA	Industrial	–	180	–	160	–	140	–	110	mA
			Commercial	-	170	-	150	-	130	-	100	mA
Standby power supply current	I_{SB}	V_{CC} = Max $\overline{CE} \geq V_{IH}$, f = Max		–	60	–	60	–	60	–	60	mA
	I_{SB1}	V_{CC} = Max $\overline{CE} \geq V_{CC} - 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$, f = 0		–	8	–	8	–	8	–	8	mA
Output voltage	V_{OL}	I_{OL} = 8 mA, V_{CC} = Min		–	0.4	–	0.4	–	0.4	–	0.4	V
	V_{OH}	I_{OH} = –4 mA, V_{CC} = Min		2.4	–	2.4	–	2.4	–	2.4	–	V

Capacitance (f = 1MHz, T_a = 25° C, V_{CC} = NOMINAL)[2]

Parameter	Symbol	Signals	Test conditions	Max	Unit
Input capacitance	C_{IN}	A, CE, WE, OE, UB, LB	V_{IN} = 0V	6	pF
I/O capacitance	$C_{I/O}$	I/O	V_{IN} = V_{OUT} = 0V	8	pF

Read cycle (over the operating range)[3,9]

Parameter	Symbol	–10		–12		–15		–20		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Read cycle time	t_{RC}	10	–	12	–	15	–	20	–	ns	
Address access time	t_{AA}	–	10	–	12	–	15	–	20	ns	
Chip enable ($\overline{CE}$) access time	t_{ACE}	–	10	–	12	–	15	–	20	ns	
Output enable ($\overline{OE}$) access time	t_{OE}	–	4	–	5	–	6	–	7	ns	
Output hold from address change	t_{OH}	3	–	3	–	3	–	3	–	ns	5
$\overline{CE}$ Low to output in low Z	t_{CLZ}	3	–	3	–	3	–	3	–	ns	4, 5
$\overline{CE}$ High to output in high Z	t_{CHZ}	–	5	–	6	–	7	–	9	ns	4, 5
$\overline{OE}$ Low to output in low Z	t_{OLZ}	0	–	0	–	0	–	0	–	ns	4, 5
$\overline{OE}$ High to output in high Z	t_{OHZ}	–	5	–	6	–	7	–	9	ns	4, 5
$\overline{LB}$, $\overline{UB}$ access time	t_{BA}	–	5	–	6	–	7	–	8	ns	
$\overline{LB}$, $\overline{UB}$ Low to output in low Z	t_{BLZ}	0	–	0	–	0	–	0	–	ns	
$\overline{LB}$, $\overline{UB}$ High to output in high Z	t_{BHZ}	–	5	–	6	–	7	–	9	ns	
Power up time	t_{PU}	0	–	0	–	0	–	0	–	ns	5
Power down time	t_{PD}	–	10	–	12	–	15	–	20	ns	5

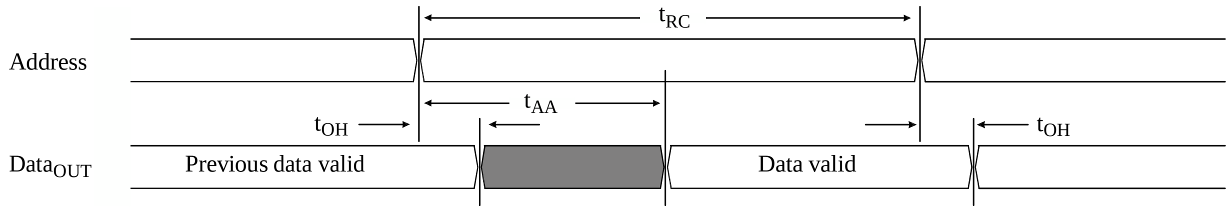
Key to switching waveforms

╱ Rising input

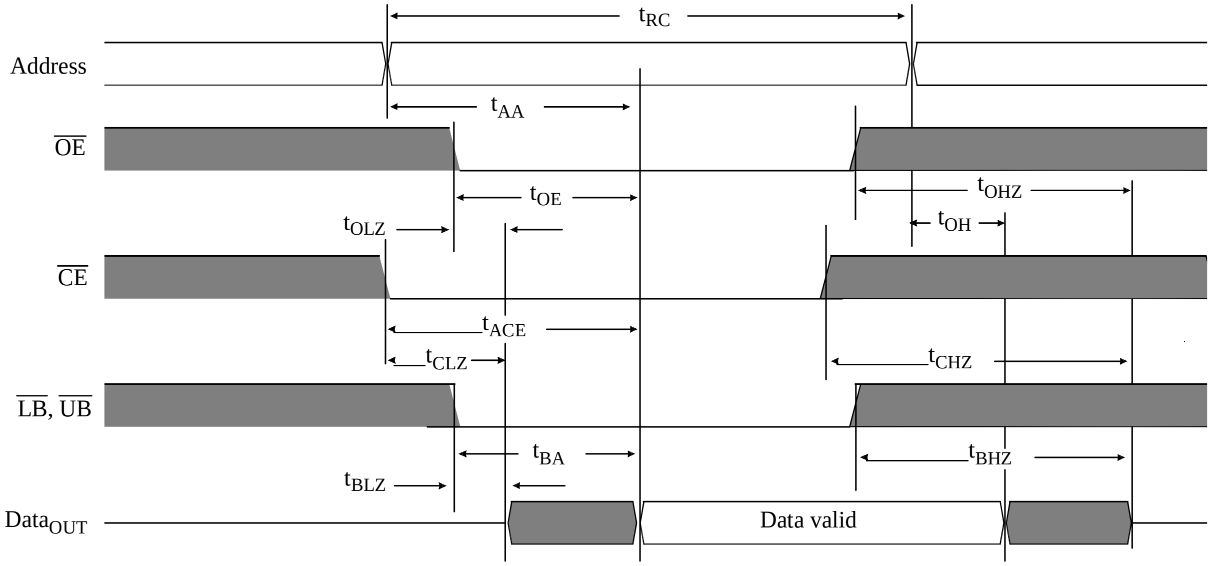
╲ Falling input

▨ Undefined/don't care

Read waveform 1 (address controlled)[6,7,9]



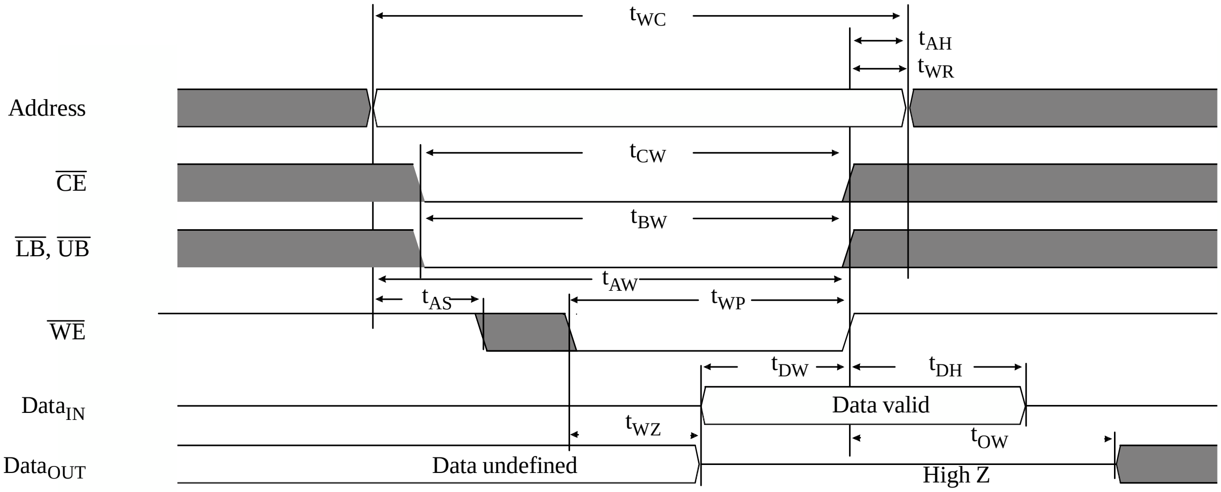
Read waveform 2 ($\overline{\text{CE}}$, $\overline{\text{OE}}$, $\overline{\text{UB}}$, $\overline{\text{LB}}$ controlled)[6,8,9]



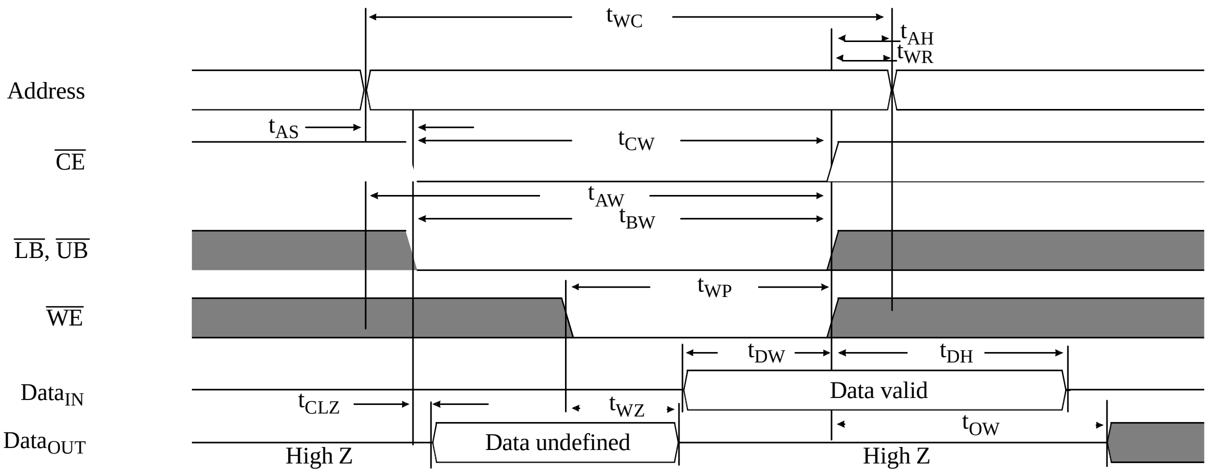
Write cycle (over the operating range)[10]

Parameter	Symbol	–10		–12		–15		–20		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Write cycle time	t_{WC}	10	–	12	–	15	–	20	–	ns	
Chip enable ($\overline{\text{CE}}$) to write end	t_{CW}	7	–	8	–	10	–	12	–	ns	
Address setup to write end	t_{AW}	7	–	8	–	10	–	12	–	ns	
Address setup time	t_{AS}	0	–	0	–	0	–	0	–	ns	
Write pulse width ($\overline{\text{OE}}$ = High)	t_{WP1}	7	–	8	–	10	–	12	–	ns	
Write pulse width ($\overline{\text{OE}}$ = Low)	t_{WP2}	10	–	12	–	15	–	20	–	ns	
Write recovery time	t_{WR}	0	–	0	–	0	–	0	–	ns	
Address hold from end of write	t_{AH}	0	–	0	–	0	–	0	–	ns	
Data valid to write end	t_{DW}	5	–	6		7	–	9	–	ns	
Data hold time	t_{DH}	0	–	0	–	0	–	0	–	ns	4, 5
Write enable to output in High-Z	t_{WZ}	0	5	0	6	0	7	0	9	ns	4, 5
Output active from write end	t_{OW}	3	–	3	–	3	–	3	–	ns	4, 5
Byte enable Low to write end	t_{BW}	7	–	8	–	10	–	12	–	ns	4, 5

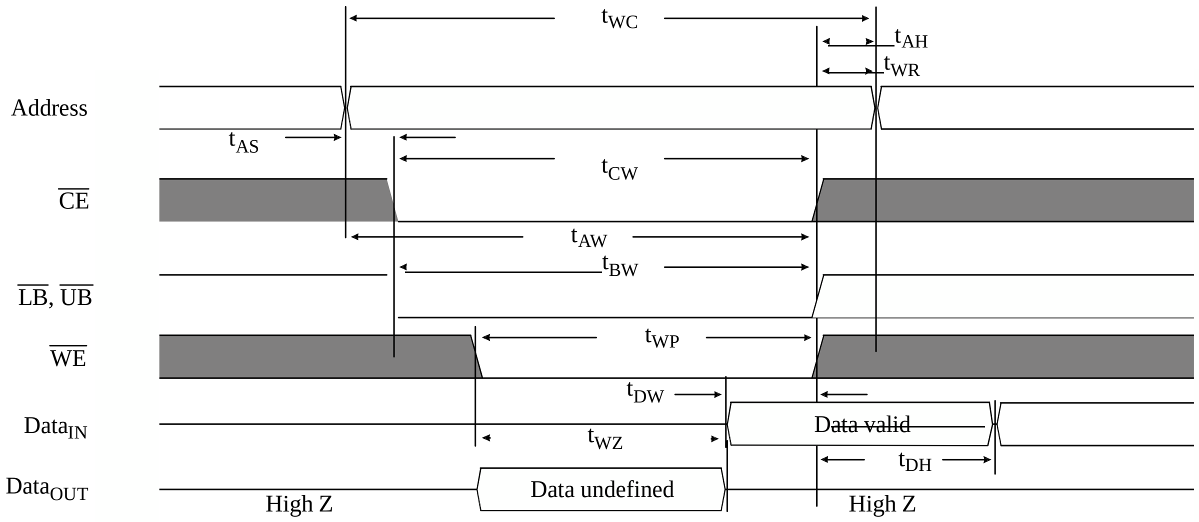
Write waveform 1($\overline{\text{WE}}$ controlled)[10]



Write waveform 2 ($\overline{\text{CE}}$ controlled)[10]



Write waveform 3 [10]



AC test conditions

- Output load: see Figure B.
- Input pulse level: GND to 3.0V. See Figure A.
- Input rise and fall times: 2 ns. See Figure A.
- Input and output timing reference levels: 1.5V.

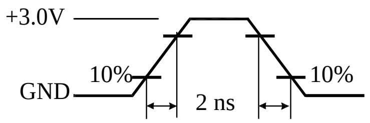


Figure A: Input pulse

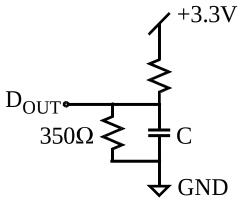
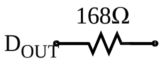


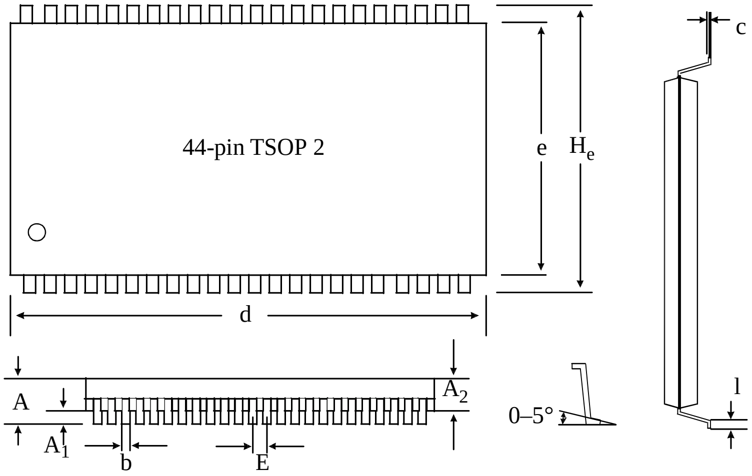
Figure B: 3.3V Output load



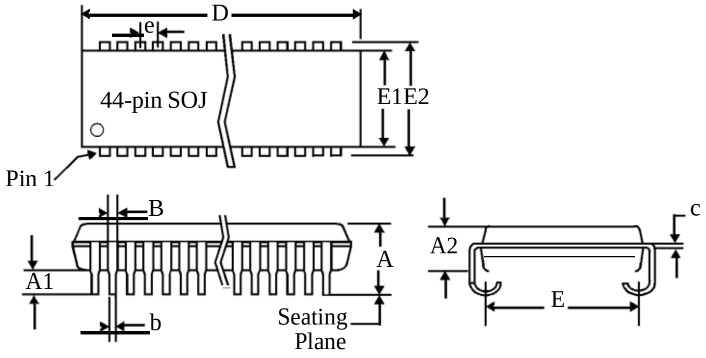
Notes

1 During V_{CC} power-up, a pull-up resistor to V_{CC} on $\overline{CE}$ is required to meet I_{SB} specification.
2 This parameter is sampled, but not 100% tested.
3 For test conditions, see *AC Test Conditions*, Figures A and B.
4 t_{CLZ} and t_{CHZ} are specified with C_L = 5pF as in Figure B. Transition is measured ±500mV from steady-state voltage.
5 This parameter is guaranteed, but not tested.
6 $\overline{WE}$ is High for read cycle.
7 $\overline{CE}$ and $\overline{OE}$ are Low for read cycle.
8 Address valid prior to or coincident with $\overline{CE}$ transition Low.
9 All read cycle timings are referenced from the last valid address to the first transitioning address.
10 All write cycle timings are referenced from the last valid address to the first transitioning address.
11 C=30pF, except on High Z and Low Z parameters, where C=5pF.

Package dimensions

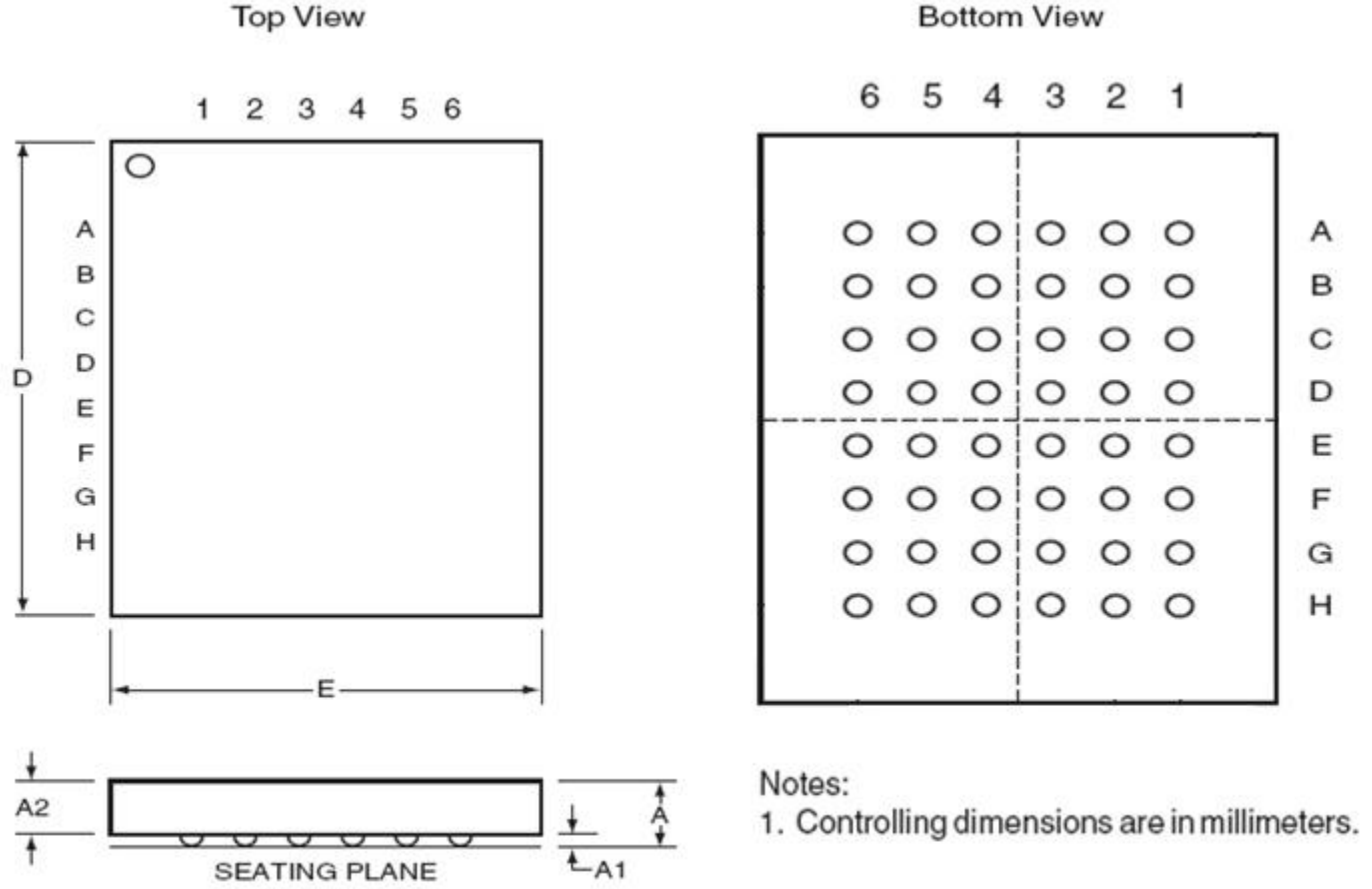


	44-pin TSOP 2	
	Min (mm)	**Max (mm)**
A		1.2
A_1	0.05	0.15
A_2	0.95	1.05
b	0.3	0.45
c	0.12	0.21
d	18.31	18.52
e	10.06	10.26
H_e	11.68	11.94
E	0.80 (typical)	
l	0.40	0.60



	44-pin SOJ 400 mils	
	Min(mils)	**Max(mils)**
A	0.128	0.148
A1	0.025	-
A2	0.105	0.115
B	0.026	0.032
b	0.015	0.020
c	0.007	0.013
D	1.120	1.130
E	0.370 NOM	
E1	0.395	0.405
E2	0.435	0.445
e	0.050 NOM	

Outline of 48BGA



Notes:
1. Controlling dimensions are in millimeters.

BGA 8mm x 10mm

	MILLIMETERS		
Sym.	Min.	Typ.	Max.
A	—	—	1.20
A1	0.24	—	0.30
A2	0.60	—	—
D	9.90	10.00	10.10
D1		5.25 BSC	
E	7.90	8.00	8.10
E1		3.75 BSC	
e		0.75 BSC	
b	0.30	0.35	0.40

Ordering Codes

Package	Temperature	10 ns	12	15 ns	20 ns
SOJ	Commercial	AS7C34098A-10JC	AS7C34098A-12JC	AS7C34098A-15JC	AS7C34098A-20JC
	Industrial	AS7C34098A-10JI	AS7C34098A-12JI	AS7C34098A-15JI	AS7C34098A-20JI
BGA	Industrial	AS7C34098A-10BIN			
TSOP 2	Commercial	AS7C34098A-10TC	AS7C34098A-12TC	AS7C34098A-15TC	AS7C34098A-20TC
	Industrial	AS7C34098A-10TI	AS7C34098A-12TI	AS7C34098A-15TI	AS7C34098A-20TI

Note: Add suffix ‘N’ to the above part numbers for Lead Free Parts. (Ex: AS7C34098A - 10TCN)

Part numbering system

AS7C	X	4098A	–XX	J / T or B	X	X
SRAM prefix	Voltage: 3 - 3.3V CMOS	Device number	Access time	Packages: J: SOJ 400 mil T: TSOP 2 B: BGA	Temperature ranges: C: Commercial, 0°C to 70°C I: Industrial, –40°C to 85°C	N = Lead Free Parts

Alliance Memory, Inc.
511 Taylor Way,
San Carlos, CA 94070
Tel: 650-610-6800
Fax: 650-620-9211
www.alliancememory.com

Copyright © Alliance Memory
All Rights Reserved
Part Number: AS7C34098A
Document Version: v. 2.2

© Copyright 2003 Alliance Memory, Inc. All rights reserved. Our three-point logo, our name and Intelliwatt are trademarks or registered trademarks of Alliance. All other brand and product names may be the trademarks of their respective companies. Alliance reserves the right to make changes to this document and its products at any time without notice. Alliance assumes no responsibility for any errors that may appear in this document. The data contained herein represents Alliance's best data and/or estimates at the time of issuance. Alliance reserves the right to change or correct this data at any time, without notice. If the product described herein is under development, significant changes to these specifications are possible. The information in this product data sheet is intended to be general descriptive information for potential customers and users, and is not intended to operate as, or provide, any guarantee or warrantee to any user or customer. Alliance does not assume any responsibility or liability arising out of the application or use of any product described herein, and disclaims any express or implied warranties related to the sale and/or use of Alliance products including liability or warranties related to fitness for a particular purpose, merchantability, or infringement of any intellectual property rights, except as express agreed to in Alliance's Terms and Conditions of Sale (which are available from Alliance). All sales of Alliance products are made exclusively according to Alliance's Terms and Conditions of Sale. The purchase of products from Alliance does not convey a license under any patent rights, copyrights; mask works rights, trademarks, or any other intellectual property rights of Alliance or third parties. Alliance does not authorize its products for use as critical components in life-supporting systems where a malfunction or failure may reasonably be expected to result in significant injury to the user, and the inclusion of Alliance products in such life-supporting systems implies that the manufacturer assumes all risk of such use and agrees to indemnify Alliance against all claims arising from such use.

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Alliance Memory:

AS7C34098A-10TCN AS7C34098A-15TCN AS7C34098A-10BIN AS7C34098A-10BINTR AS7C34098A-12JCN AS7C34098A-12TCN AS7C34098A-12TIN AS7C34098A-10JIN AS7C34098A-15JIN AS7C34098A-12JINTR AS7C34098A-15TIN AS7C34098A-15JCN AS7C34098A-10TINTR AS7C34098A-15JINTR AS7C34098A-10TIN AS7C34098A-20TCNTR AS7C34098A-20JCNTR AS7C34098A-10JINTR AS7C34098A-20JINTR AS7C34098A-10TCNTR AS7C34098A-12TCNTR AS7C34098A-20TIN AS7C34098A-12JCNTR AS7C34098A-20JCN AS7C34098A-15TINTR AS7C34098A-10JCNTR AS7C34098A-20TCN AS7C34098A-20TINTR AS7C34098A-12TINTR AS7C34098A-15JCNTR AS7C34098A-10JCN AS7C34098A-15TCNTR AS7C34098A-12JIN AS7C34098A-20JIN